# San José State University
# Electrical Engineering Department
# EE256, DSP Architectures, Sec. 1, Spring 2013

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| **Instructor:** | Avtar Singh |
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| **Office Hours:** | MW: 14:00-14:50, T: 14:00-16:00 + by appointment |
| **Class Days/Time:** | MW 19:30-20:45 |
| **Classroom:** | Eng 403 |
| **Prerequisites:** | EE210 |

## Course Description

Implementations of DSP algorithms using programmable DSP architectures, internal DSP architectural requirements for a DSP device, system level hardware/ software design, and applications of DSP architectures.

## Required Material

Text: Singh, A. and Srinivasan, S., Digital Signal Processing, Thomson, 2004
Development Board: eZDSP5505

## Course Goals and Student Learning Objectives

| | **Student Learning Objective (SLO)** | ***Program Outcomes (POs)** |
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| 1. | Ability to analyze DSP algorithms and operations for a DSP processor implementations | 1, 2 |
| 2. | Ability to use MATLAB for DSP analysis and design | 1, 2, 3 |
| 3. | Ability to determine architecture and hardware to implement DSP operations and algorithms | 1, 2 |
| 4. | Ability to analyze a programmable DSP device | 1, 2 |

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| 5. | Ability to understand software model for a DSP device | 1, 2 |
| 6. | Ability to use DSP software development tools | 3 |
| 7. | Ability to implement DSP algorithms for filters and controllers | 1, 2, 3 |
| 8. | Ability to develop assembly code for a digital filter | 1, 2, 3 |
| 9. | Ability to understand interfacing serial converters to a programmable DSP device | 1, 2 |
| 10. | Ability to analyze synchronous serial interface | 1, 2 |
| 11. | Ability to program a multi-channel buffered serial port | 1, 2, 3 |
| 12. | Ability to implement a real-time DSP scheme | 1, 2, 3 |
| 13. | Ability to evaluate computational accuracy of DSP implementations | 1, 2 |
| 14. | Ability to understand quantization, truncation, rounding, overflow, and saturation errors in DSP implementations | 1, 2 |
| 15. | Ability to implement FFT algorithms for spectrum analysis | 1, 2, 3 |
| 16. | Ability to interface memory to a programmable DSP device | 1, 2 |
| 17. | Ability to interface data converters to a programmable DSP device | 1, 2 |

***Program Outcomes (POs)**

1) Students will be able to base analysis, problem solving and design on core advanced EE theory.
2) Students will be able to develop deeper understanding of an area of concentration in their graduate programs.
3) Students will be able to apply modern tools for computations, simulations, analysis, and design.
4) Students will be able to communicate engineering results effectively.

**Grading**

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| Homework/ Labs | 20% |
| Midterm Exam | 20% |
| Final Exam | 30% |
| Lab Project | 30% |

Standard grading method will be used to assign letter grades. For instance an overall score of 90% will be assigned a letter grade of A-. Any adjustment to this scheme of grading, if necessary, will be described in the class.

**Examinations**

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| **Midterm:** | **Class Announcement** |
| **Final:** | **University Schedule** |

## Dropping and Adding

Students are responsible for understanding the policies and procedures about add/drops, academic renewal, etc. Information on add/drops are available at http://info.sjsu.edu/web-dbgen/narr/soc-fall/rec-298.html. Information about late drop is available at http://www.sjsu.edu/sac/advising/latedrops/policy/ **.** Students should be aware of the current deadlines and penalties for adding and dropping classes.

## Assignments and Grading Policy

Assignments, homeworks, and projects grading will be described in the class. In general late submissions will not be accepted. Attendance per se shall not be used as a criterion for grading according, however, student will be held responsible for all announcements made during the class.

## University Policies

### Academic integrity

Students should know that the University's Academic Integrity Policy is availabe at http://www.sa.sjsu.edu/download/judicial_affairs/Academic_Integrity_Policy_S07-2.pdf. Your own commitment to learning, as evidenced by your enrollment at San Jose State University and the University's integrity policy, require you to be honest in all your academic course work. Faculty members are required to report all infractions to the office of Student Conduct and Ethical Development. The website for Student Conduct and Ethical Development is available at http://www.sa.sjsu.edu/judicial_affairs/index.html.

Instances of academic dishonesty will not be tolerated. Cheating on exams or plagiarism (presenting the work of another as your own, or the use of another person's ideas without giving proper credit) will result in a failing grade and sanctions by the University. For this class, all assignments are to be completed by the individual student unless otherwise specified. If you would like to include in your assignment any material you have submitted, or plan to submit for another class, please note that SJSU's Academic Policy F06-1 requires approval of instructors.

### Campus Policy in Compliance with the American Disabilities Act

If you need course adaptations or accommodations because of a disability, or if you need to make special arrangements in case the building must be evacuated, please make an appointment with me as soon as possible, or see me during office hours. Presidential Directive 97-03 requires that students with disabilities requesting accommodations must register with the DRC (Disability Resource Center) to establish a record of their disability.

# EE256, DSP Architectures and Applications, Spring 2013, Course Schedule

*This schedule is subject to change. Any required change will be discussed in class.*

| Week | Topics, Readings, Assignments, Deadlines |
|---|---|
| 1, 2 | **Introduction to Digital Signal Processing Operations (Chapter 2)**<br>The Sampling Theorem and Digital Signal Sequences<br>Frequency Response and FIR/ IIR Filters<br>DFT and FFT<br>Computer Based Tools for DSP Analysis and Design<br>Homework/Lab*: Using MATLAB for DSP Analysis and Design* |
| 3, 4 | **Architectural Requirements of a DSP Device (Chapter 4)**<br>Architectures and hardware to implement DSP operations and algorithms<br>Comparison of various DSP architectures in use<br>Homework |
| 5, 6 | **Programmable DSP Devices (Chapter 5)**<br>Architectural Analysis of a DSP Device<br>The Instruction Set and the Addressing Modes<br>Writing Assembly Code for Applications<br>Homework |
| 7 | **MIDTERM EXAM** |
| 8 | **DSP Implementation Tools (Chapter 6)**<br>DSP Software Development Tools: Compiler, Assembler, Linker, Simulator, and Debugger<br>Homework/Lab*: Using TMS320C5000 Software Development Tools* |
| 9, 10 | **Software Implementations of DSP Algorithms (Chapter 7)**<br>Assembly Code Implementations: FIR Filters, IIR Filters, Interpolation Filters, Decimation Filters, PID Controllers, Adaptive Filters, and Nonlinear Operations.<br>Homework/Lab*: Developing Assembly Code for a Digital Filter* |
| 11, 12 | **Interfacing Serial Converters to a Programmable DSP Device (Chapter 10)**<br>Synchronous Serial Interface between the DSP and an AIC<br>A Multi-channel Buffered Serial Port (McBSP)<br>The McBSP Programming<br>An Analog Interface Circuit (AIC)<br>Homework/ Lab Project*: Implementing and Demonstrating a Real-time DSP Scheme* |
| 13 | **Computational Accuracy in DSP Implementations (Chapter 3)**<br>The DSP System Model<br>Quantization, Truncation, Rounding, Overflow, and Saturation Errors in DSP Implementations |

| Week | Topics, Readings, Assignments, Deadlines |
|---|---|
| | Homework |
| 14, 15 | **Software Implementations of FFT Algorithms (Chapter 8)**<br>Spectrum Analysis<br>Homework/ Lab Project*:* *Implementing an FFT Algorithm for Spectrum Analysis* |
| 16 | **Interfacing Memory and Peripherals to DSP Devices (Chapter 9)**<br>Memory Interfacing, A/D and D/A Interfacing<br>Homework |
| | **FINAL EXAM (University Schedule)** |