San José State University
College of Engineering/Electrical Engineering
EE226, VLSI Technogy
Spring 2012

Instructor:	**Lili He**
Office Location:	ENG 357
Telephone:	(408) (924-4073)
Email:	lili.he@sjsu.edu
Office Hours:	TR 10:15-12:00pm, and 2:00-2:45pm
Class Days/Time:	TR 3:00-4:15pm
Classroom:	DMH 149A
Prerequisites:	EE221 or Consent of instructor

Course Description

This course is a continuation of EE221 study in semiconductor device technology. The course will cover the following: introduction to CMOS/BiCMOS technologies for VLSI circuits; theoretical and practical aspects of individual fabrication steps; necessity of particular steps in order to achieve required device/circuit parameters; tradeoffs in optimizing device performance; microprocessor technologies; high density CMOS memory design projects using various simulation programs and IC layout techniques.

Course Goals and Student Learning Objectives

Upon successful completion of this course, students will be able to:

LO1 **Describe** fundamental concepts of semiconductor devices fabraction by Silicon and compound semiconductor materials.

LO2 **Explain** basic principles of device fabrication

LO3 **Illustrate** basic VLSI fabrication technology

Required Texts/Readings

Textbook

Semiconductor Devices: Physics and Technology 2nd ed., by S.M.Sze, John Wiley, 2002, ISBN0471333727

Other Readings

1. Silicon VLSI Technology J.D. Plummer, M.D. Deal, P. B. Griffin, Printice Hall, 2000
2. Physics and Technology of Semiconductor Devices, A.S. Grove, John Wiley, 1967.
3. Device Electronics for Integrated Circuits, RS. Muller and T.I. Kamins, John Wiley, 1977.
4. VLSI Fabrication Principles, Sorab K. Ghandi, John Wiley, 1983.
5. VLSI Technology, S.M. Sze, McGraw- Hill, 1985.
6. Microelectronic Processing- An Introduction to Manufacturing Integrated Circuits, W. Scott Ruska, McGraw- Hill, 1987.
7. Electronic Materials Science for Integrated Circuits in Si and GaAs, Shyam P. Murarka and Martin C. Peckerer, Academic Press, 1989.
8. Electronic materials Science and Technology, James W. Mayer and S.S. Lau, Macmillan, 1990.

Classroom Protocol

Students are expected to participate actively in class. Students will turn their cell phones off or put them on vibrate mode while in class. They will not answer their phones in class.

Assignments and Grading Policy

a) One middle term and one final exam
b) Homework: There will be one homework assignment for each chapter. Solutions will be posted in my web page one week after each chapter lectures. Homework will not be collected.
c) Project(report and presentation): Topics related to semiconductor technology will be provided. Students chose one topic from the list. Report and in class presentation are required. Detailed guideline for project will be distributed later in class.

Dropping and Adding

Students are responsible for understanding the policies and procedures about add/drops, academic renewal, etc. Information on add/drops are available at http://info.sjsu.edu/web-dbgen/narr/soc-fall/rec-298.html. Information about late drop is available at http://www.sjsu.edu/sac/advising/latedrops/policy/ . Students should be aware of the current deadlines and penalties for adding and dropping classes.

Grading Policy:

Project report	**20%**
Project presentation	**20%**
Middle term exam	**25%**
Final exam	**35%**

Final Grade Percentage Breakdown

90% and above	A
89% - 85%	A-
84% - 80%	B+
79% - 70%	B
69% - 65%	B-
64% - 60%	C+
59% - 55%	C
54% - 50%	C-
49% - 45%	D+
44% - 40%	D
below 40%	F

University Policies

Academic integrity

Students should know that the University's Academic Integrity Policy is availabe at http://www.sa.sjsu.edu/download/judicial_affairs/Academic_Integrity_Policy_S07-2.pdf. Your own commitment to learning, as evidenced by your enrollment at San Jose State University and the University's integrity policy, require you to be honest in all your academic course work. Faculty members are required to report all infractions to the office of Student Conduct and Ethical Development. The website for Student Conduct and Ethical Development is available at http://www.sa.sjsu.edu/judicial_affairs/index.html.

Instances of academic dishonesty will not be tolerated. Cheating on exams or plagiarism (presenting the work of another as your own, or the use of another person's ideas without giving proper credit) will result in a failing grade and sanctions by the University. For this class, all assignments are to be completed by the individual student unless otherwise specified. If you would like to include in your assignment any material you have submitted, or plan to submit for another class, please note that SJSU's Academic Policy F06-1 requires approval of instructors.

Campus Policy in Compliance with the American Disabilities Act

If you need course adaptations or accommodations because of a disability, or if you need to make special arrangements in case the building must be evacuated, please make an appointment with me as soon as possible, or see me during office hours. Presidential Directive 97-03 requires that students with disabilities requesting accommodations must register with the DRC (Disability Resource Center) to establish a record of their disability.

EE226 / VLSI Technology, Section-1
Spring 2012, Course Schedule

Table 1 Tentative Course Schedule
The schedule is subject to change with fair notice to be announced in class.

Tentative Class Schedule:

Week	Topic	Reading	Home Work Assignment
1/26	Introduction to semiconductor devices and technology	Chapter 1	
1/31 & 2/2	CMOS technology	Chap. 2 (Plummer) & Chap 6 (Sze)	
2/7 & 2/9	Crystal Growth and Epitaxy	Chapter 10	
2/14 & 2/16	Crystal Growth and Epitaxy, Film Formation	Chapter 10, 11	Chap. 10: 3,9,12,14,15
2/21 & 2/23	Film Formation	Chapter 11	Chap. 11: 1,4,6,7,14,17
2/28 & 3/1	Lithography and Etching	Chapter 12	
3/6 & 3/8	**Middle term exam**		
3/13 & 3/15	Lithography and Etching	Chapter 12	Chap. 12: 3,9,11,17
3/20 & 3/22	Impurity Doping	Chapter 13	Chap. 13; 1,3,6,10,13,16
3/26-3/30	Spring Recess		
4/3 & 4/5	Integrated Devices	Chapter 14	Chap. 14: 2, 6, 8, 10, 19
4/10 &4/12	Recent Progresses in VLSI technology	Class Notes	
4/17 & 4/19	Recent Progresses in VLSI technology	Class Notes	
4/24 & 4/26	Student project presentation		
5/1 & 5/3	Student project presentation		
5/8 & 5/10	Student project presentation		
5/15	**Review for finals**		
	Final Exam: Wednesday, 5/23, 2:45-5:00pm		

San Jose State University

Electrical Engineering Department

EE Department Honor Code

The Electrical Engineering Department will enforce the following Honor Code that must be read and accepted by all students.

"I have read the Honor Code and agree with its provisions. My continued enrollment in this course constitutes full acceptance of this code. I will NOT:

- *Take an exam in place of someone else, or have someone take an exam in my place*
- *Give information or receive information from another person during an exam*
- *Use more reference material during an exam than is allowed by the instructor*
- *Obtain a copy of an exam prior to the time it is given*
- *Alter an exam after it has been graded and then return it to the instructor for re-grading*
- *Leave the exam room without returning the exam to the instructor."*

Measures Dealing with Occurrences of Cheating

- *Department policy mandates that the student or students involved in cheating will receive an "F" on that evaluation instrument (paper, exam, project, homework, etc.) and will be reported to the Department and the University.*
- *A student's second offense in any course will result in a Department recommendation of suspension from the University.*