San José State University
Electrical Engineering Department
EE229, Advanced Topics in Microelectronics , Spring 2011

Instructor: Morris Jones
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Office Hours: Tu, Th 2-4PM Other days by appointment
Class Days/Time: Tu,Th 4:30PM - 5:45PM
Classroom: IS113

Prerequisites:
EE227, 223, or other circuits class (RFID, etc.)

Web Page

Http://www.engr.sjsu.edu/mjones
Desire2 learn link https://sjsu.desire2learn.com/

Course Description

EE229 is a project class. Industry tools will be used to illustrate principles taught. Overall concepts will be tied together by a design project. Project team work will be stressed.

Course Goals and Student Learning Objectives

- Prepare students to be productive members of an industrial CMOS design team
- Prepare students for graduate projects involving mixed signal circuits
- Provide an understanding of the BSIM 4 transistor
- Provide an opportunity developing teamwork skills
- Provide an environment where students learn to think critically
- Provide an environment where students learn to enjoy the learning and designing process
- Have students internalize the culture of the design engineer

Course Objectives (Outcomes):

To be productive members of an industrial mixed signal design team, students should be able to:

- Practice and demonstrate critical thinking
- Understand requirements and translate them to a circuit design
- Understand capabilities and limitations of CMOS transistors and adjust designs to best use

CMOS technologies.

- Demonstrate an ability to use industry tools to achieve desired project objectives.
- Discuss design issues with future employers

Critical thinking has been described as:

A person who thinks critically can ask appropriate questions, gather relevant information, efficiently and creatively sort through this information, reason logically from this information, and come to reliable and trustworthy conclusions about the world that enable one to live and act successfully in it. ... critical thinking mimics the well-known method of scientific investigation: a question is identified, an hypothesis formulated, relevant data sought and gathered, the hypothesis is logically tested and evaluated ... [1]

Students who can think critically can:

- Determine what information is required to achieve an objective, find that information, and apply it
- Create designs from limited information
- design test benches that can prove that a design meet a specification
- identify design errors, and adjust a design to meet specifications
- Ask meaningful questions when seeking help.

A course goal is students learn to enjoy the CMOS ASIC design team experience through a *hands on* approach.

Student Preparedness

Students are expected to have previously taken a course covering CMOS devices and circuit design. Students will be given a vague specification for the design project, and are expected to perform research and form clarifying questions to complete the project.

Outcome Assessment (Grading):

- Homework (10%): Homework will consist of a mix of analysis and design problems. Analytical and CAD based techniques will be required to solve problems. The homework is designed to reinforce lecture concepts and prepare the student for the exams and class project. Homework assignments will be due according to the green sheet. Students are expected to maintain a blog of project related issues on desire2learn. They are required to make an entry every week for full credit. Students are expected to research at least one circuits related topic, and make a class presentation during the semester.
    - All homework shall be submitted on the desire2learn system. (you can access the system at https://sjsu.desire2learn.com/
        - You can scan paper documents at the academic success center
    - Developing professional discipline such as on time homework submission is expected and required. The Desire2learn system will not inform you an assignment is late. Homework scores are prorated according to the following schedule:
        - 100% Earned score Early or on time
        - 0% Earned score Late (Not accepted late)
- Midterm (35%): Covers the first half of the semester. All EE229 exams are closed book, no notes. Scratch paper will be provided during the exam. You will be seated randomly in the class, and there will be multiple versions of the exam. (depending on class size). You should bring a calculator and writing instruments to the exam. Programmable calculators are not allowed. Each exam version is normalized to the high score on that version to provide fairness. Photo ID is required when you turn in your exam.
- Final Exam (55%): The final exam will be your project submission. The project requires design and simulation. Layout will not be required in EE229, but may be performed. Students will submit the project report, and make a 10-15 minute presentation of results during the final exam period. The presentation will be graded and become part of the project score.

Grading Scale

Grade	%	Comment
A	100%	May vary down from 100%
A-	90 – 99.999%	May vary down from 99.999%
B/+/-	80-89.9999%	varies for + and -
C+	78-79.99999%	No C or C- grades are typically given graduate students in EE229.
F	0-77.99999%	

The +/- grade breaks are set by adjusting the thresholds up and down to meet the department grade distribution guidelines. The break points will not be known until the semester is over, and the class composite scores are available.

Honor Code

Your commitment as a student to learning is evidenced by your enrollment at San Jose State University. The University's Academic Integrity policy, located at http://www.sjsu.edu/senate/S07-2.htm, requires you to be honest in all your academic course work. Faculty members are required to report all infractions to the office of Student Conduct and Ethical Development. The Student Conduct and Ethical Development website is available at http://www.sa.sjsu.edu/judicial_affairs/index.html.

Instances of academic dishonesty will not be tolerated. Cheating on exams or plagiarism (presenting the work of another as your own, or the use of another person's ideas without giving proper credit) will result in a failing grade and sanctions by the University. For this class, all assignments are to be completed by the individual student unless otherwise specified. If you would like to include your assignment or any material you have submitted, or plan to submit for another class, please note that SJSU's Academic Policy S07-2 requires approval of instructors.

San Jose State University
Electrical Engineering Department
EE Department Honor Code

The Electrical Engineering Department will enforce the following Honor Code that must be read and accepted by all students.

"I have read the Honor Code and agree with its provisions. My continued enrollment in this course constitutes full acceptance of this code. I will NOT:

- *Take an exam in place of someone else, or have someone take an exam in my place*
- *Give information or receive information from another person during an exam*
- *Use more reference material during an exam than is allowed by the instructor*
- *Obtain a copy of an exam prior to the time it is given*
- *Alter an exam after it has been graded and then return it to the instructor for re-grading*
- *Leave the exam room without returning the exam to the instructor."*

Measures Dealing with Occurrences of Cheating

- *Department policy mandates that the student or students involved in cheating will receive an "F" on that evaluation instrument (paper, exam, project, homework, etc.) and will be reported to the Department and the University.*

A student's second offense in any course will result in a Department recommendation of suspension from the University.

Dropping and Adding

Students are responsible for understanding the policies and procedures about add/drop, grade forgiveness, etc. Refer to the current semester's Catalog Policies section at http://info.sjsu.edu/static/catalog/policies.html. Add/drop deadlines can be found on the current academic calendar web page located at http://www.sjsu.edu/academic_programs/calendars/academic_calendar/. The Late Drop Policy is available at http://www.sjsu.edu/aars/policies/latedrops/policy/**.** Students should be aware of the current deadlines and penalties for dropping classes.

Information about the latest changes and news is available at the Advising Hub at http://www.sjsu.edu/advising/.

Classroom Protocol

Students will turn their cell phones off or put them on vibrate mode while in class. They will not answer their phones in class. Students whose phones disrupt the course and do not stop when requested by the instructor will be referred to the Judicial Affairs Officer of the University.

Campus Policy in Compliance with the American Disabilities Act

If you need course adaptations or accommodations because of a disability, or if you need to make special arrangements in case the building must be evacuated, please make an appointment with me as soon as possible, or see me during office hours. Presidential Directive 97-03 requires that students with disabilities requesting accommodations must register with the DRC (Disability Resource Center) to establish a record of their disability.

Course plan

The following are the intended topics for discussion. The class often gets ahead of the following topics, and then reviews.

The items labeled QUIZ are desire2learn quizzes (online quizzes) each students should perform outside of class online. The items labeled HW are homework assignments. The homework assignments can be found and are turned in on the desire2learn system http://sjsu.desire2learn.com

Date	Topic	assignments
Jan 27	Introduction, class overview	
Feb 01	The BSIM transistor	
Feb 03	GM-RDS – The challenge	
Feb 08	Project proposal discussion	
Feb 10	Designing for RDS	Project proposal first draft
Feb 15	Delta sigma overview	
Feb 17	Verilog AMS overview	
Feb 22	Verilog AMS test bench concepts	Project proposal final
Feb 24	Verilog AMS examples	
Mar 01	Project discussions	
Mar 03	Mixed signal test benches	
Mar 08	Lab review	Progress report

Date	Topic	assignments
Mar 10	PLL feedback loops	
Mar 15	PLL feedback loops	
Mar 17	Midterm Review	Study Guide
Mar 22	Midterm	
Mar 24	Delta-sigma design	
Mar 29	Spring Break	
Mar 31	Spring Break	
Apr 05	Delta-sigma design – higher order	
Apr 07	Lab review	VerilogA Simulation Model
Apr 12	Student report	
Apr 14	Lab review	
Apr 19	Student report	
Apr 21	Lab review	Progress report
Apr 26	Student report	
Apr 28	Lab review	
May 03	Debugging mixed signal designs	Rough draft final report
May 05	Lab review	
May 10	Debugging mixed signal designs	
May 12	Lab review	
May 17	Final Review	
May xx	Final	

Text Book

There is no text book for EE229. It is taught from notes, and lecture materials.

Students are expected to locate and download the following materials:

- BSIM 4 manual
- VerilogA LRM
- delta-sigma matlab toolkit