EE 225a: Analog IC Transistor Process Design

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Course Description:
Advanced process design, fabrication and testing of transistors for analog integrated circuits, design of statistical process control procedures for yield management, industry standard TCAD tools (Synopsys) and IC fabrication equipment will be used extensively in lab.

This is a team-oriented, interdisciplinary course enrolling EE, MatE, ChE, ME, Chemistry and Physics majors. Each student brings a different background to the course. The laboratory is the central theme of the course. This course will require a considerable amount of work outside of regularly scheduled class time so be prepared to invest a lot of time.

SPC Overview: This part of the laboratory is intended to demonstrate the basics of Statistical Process Control, for variable and attribute control charting. This includes the statistical background, how to prepare and properly monitor charts, some of the potential pitfalls for chart use, and other topics as time permits. The student will be given to opportunity to perform several analyses to ensure that the concepts presented are maintained. One midterm and one mini-final (for the section) will be given, as announced in class.

Students will complete three major team projects:

- A design of a 2-mask MOS or solar cell process
- SPC project on overlay alignment in a photolithography system.
- Fabrication and test of a 2-mask MOS process
- Testing MOS-based Analog circuits\
- SPC techniques will be used in each project to explain results and make recommendations.

Prerequisites:

All students must have had at least a graduate level device physics course such as EE221.

Course Aims:

Students should know at the end of this course:

1. CMOS Analog Circuit Design/testing
2. CMOS Processing modeling
3. T-CAD Modeling
4. Metrology
5. Team Work
6. Process Control

Outcome Assessment (Grading):

There is no curve; the numerical values will directly translate in to a 0 to 4 scale from a 0 to 100 scale. Given that this course is still under development this grading scale is an estimate of what will be assessed. If it is determined that a project can not be completed, due to equipment failures, or some unforeseen problem with lab, then the rest of the points will be evenly distributed over the rest of the projects.

Oral and written reports will be assessed on content and proper format. Oral and written reports that are incomplete (for example lacking an abstract or an analysis section) will receive a 0 for the entire report.

If it is determined that various teams members are not participating in lab, a lab practical will be given on the various skills required to complete the projects. If a student receives a NO-GO on a supporting skill, then the student's grade will be lowered by a minimum of 20%. If the non-participation problem continues the team member who is no participating will be re-assigned to another group.

If a student misses or is late for a laboratory with out consulting with the team leader or me, the student's grade will be lowered by 5% on the current project.

There are many chances to earn extra credit. Team leaders that excel, or team members that contribute an extra amount can receive up to 5% extra on their final grade.

The letter I indicates an individual grade and the letter G indicates a group grade. Individual grades will be moved down if it is shown that a team member is not participating.

Surprise quizzes will be administered to test whether or not a student has prepared by reading the material or coordinated with the team members. Failure on a quiz will reduce the student's grade by 20% for that day's activities.

- Homework (18%)

- Final (15%)
- Process Design with TCAD (Sentaurus) (23%): Student teams will
    - Learn/review the Sentaurus CAD software (I, 3%):
        - Unix CDS tutorial (I, 2%)
        - Completing a Tutorial
        - Modifying a sub-micron MOSFET process file to shift VTO from one specification to another
    - Design a two MASK NMOS, given a template file (G, 10%). Oral presentation with a poster detailing their design.
    - Students will write a detailed traveler for their design (G, 10%).
- SPC Project (10%): student teams will
    - Collect and analyze registration overlay error and create a written report with control charts and recommendations for design rules and modifications to the two-mask process designed in the Athena project (G).
- Fabrication Project (10%) (G): Students will fabricate and test their two-mask process. They will present their results in a written report. Student will explain their results in terms of their SPC data.
- Analog IC Design/Test Project (24%):
    - Student teams will design/test analog circuits. (G):
    - Students will fabricate and test their designs and present their work

The schedule is a guide!!!!

#	Date	Topic	Read	Items Due	
1	1/22/2009	Device Physics Review 1	Notes		
2	1/27/2009	Device Physics Review 1	Notes	HW 1	Review, Diagnostic
3	1/29/2009	Design of CMOS Analog Circuits 1	Notes		
4	2/3/2009	Design of CMOS Analog Circuits 2	Notes	HW 2	Design Current Mirror
5	2/5/2009	SPC 1	6.1/6.2		
6	2/10/2009	Tape Out Projects	NA	HW 3	6.1 , 6.6
7	2/12/2009	SPC 2	6.3		
8	2/17/2009	SPC 3	6.4		
9	2/19/2009	Review of Semiconductor Manufacturing	1	HW 4	Sample Control Charts
10	2/24/2009	Oxidation	2.1	HW 5	# 1.1, 1.2, 1.3
11	2/26/2009	Photolithography	2.2		
12	3/3/2009	Etching	2.3	HW 6	#2.1, 2.2 2.3
13	3/5/2009	Doping	2.4		
14	3/10/2009	Transistor Process Design	Notes	HW 7	#2.4, 2.6, 2.7
15	3/12/2009	Project Design Reviews			
16	3/17/2009	Yield 1	5.1/5.2		
17	3/19/2009	Yield 2	5.3/5.4		
18	3/24/2009	Spring Break			
19	3/26/2009	Spring Break			
20	3/31/2009	Holiday			
21	4/2/2009	Continue two mask fabrication project		HW 8	#5.1, 5.2, 5.3
22	4/7/2009	Reliability 1	Notes		
23	4/9/2009	Continue two mask fabrication project			
24	4/14/2009	Reliability 2	Notes		
25	4/16/2009	Continue Testing	Testing Manual		
26	4/21/2009	Statistical Experimental Design 1	7.1		
27	4/23/2009	Continue Testing	Testing Manual		
28	4/28/2009	Statistical Experimental Design 2	7.2		
29	4/30/2009	Statistical Experimental Design 3	7.3	HW 9	#7.1, 7,2
30	5/5/2009	CMOS Review	Notes		
31	5/7/2009	Continue Testing	Testing Manual		
32	5/12/2009	SPC Review	Notes		
33	5/21/2009	Final Exam 14:45-1700			

Textbooks:

Required:

R. C. Jaeger, Introduction to Microelectronic Fabrication, 2nd edition, Prentice Hall, 2002, ISBN 0-20144494-1

Additional:

- Wolf & R.N. Tauber, Silicon Processing for the VLSI Era: Volume 1-Process Technology, 2nd edition, Lattice Press, 2000. Available at Spartan Bookstore
- E. L. Grant and R. Leavenworth, Statistical Quality Control, ISBN 0-07-844354-7
- Spartan Semiconductor Employee Handbook. Available at Maple Press, 481 E San Carlso Street, San Jose; 408-297-1001
- Ghandhi, S.K. VLSI Fabrication Principles, Wiley 1983.

Lab Activities (Note this is subject to change):

#	Date	Topic	Item Due
1	1/22/2009	Unix Tutorial Sentaurus Si Bar Tutorial	
2	1/29/2009	Sprocess Tutorial	
3	2/5/2009	Develop MIS Process Recipe	
4	2/12/2009	Lab Training Day	
5	2/19/2009	FABRICATE MIS	
6	2/26/2009	TEST MIS Capacitor	
7	3/5/2009	SPC Project	
8	3/12/2009	Refine MIS Process	
9	3/19/2009	Design 4 Mask Process	
10	3/26/2009	Spring Break	
11	4/2/2009	Start 4 mask fabrication project	
12	4/9/2009	Continue 4 mask fabrication project	
13	4/16/2009	Continue 4 mask fabrication project	
14	4/23/2009	Testing 4 mask project	
15	4/30/2009	Testing Analog IC design	
16	5/7/2009	Testing Analog IC design	
17	5/14/2009	Lab Cleanup	

Grading Percentage Breakdown

94% and above	A
93% - 90%	A-
89% - 87%	B+
86% - 84%	B
83% - 80%	B-
79% - 77%	C+
76% - 74%	C
73% - 70%	C-
69% - 67%	D+
66% - 64%	D
63% - 60%	D-
below 60%	**F**

Extra credit options:
There will be opportunities to earn extra credit. For example one might attend the ISSC conference or various on campus activities or have the best project for the semester. There will be no extra credit given after the final exam.

Eating:
Eating and drinking (except water) are prohibited in the Boccardo Business Center. Students with food will be asked to leave the building. Students who disrupt the course by eating and do not leave the building will be referred to the Judicial Affairs Officer of the University.

Cell Phones:
Students will turn their cell phones off or put them on vibrate mode while in class. They will not answer their phones in class. Students whose phones disrupt the course and do not stop when requested by the instructor will be referred to the Judicial Affairs Officer of the University.

Computer Use:
In the classroom, faculty allow students to use computers only for class-related activities. These include activities such as taking notes on the lecture underway, following the lecture on Web-based PowerPoint slides that the instructor has posted, and finding Web sites to which the instructor directs students at the time of the lecture. Students who use their computers for other activities or who abuse the equipment in any way, at a minimum, will be asked to leave the class and will lose participation points for the day, and, at a maximum, will be referred to the Judicial Affairs Officer of the University for disrupting the course. (Such referral can lead to suspension from the University.) Students are urged to report to their instructors computer use that they regard as inappropriate (i.e., used for activities that are not class related).

Academic Honesty:
Faculty will make every reasonable effort to foster honest academic conduct in their courses. They will secure examinations and their answers so that students cannot have prior access to them and proctor examinations to prevent students from copying or exchanging information. They will be on the alert for plagiarism. Faculty will provide additional information, ideally on the green sheet, about other unacceptable procedures in class work and examinations. Students who are caught cheating will be reported to the Judicial Affairs Officer of the University, as prescribed by Academic Senate Policy S04-12.

"You are responsible for understanding the policies and procedures about add/drops, academic renewal, withdrawal, etc. found at http://www2.sjsu.edu/senate/S04-12.pdf

• Expectations about classroom behavior; see Academic Senate Policy S90-5 on Student Rights and Responsibilities.

• As appropriate to your particular class, a definition of plagiarism, such as that found on Judicial Affairs website at http://www2.sjsu.edu/senate/plagarismpolicies.htm

• "If you would like to include in your paper any material you have submitted, or plan to submit, for another class, please note that SJSU's Academic Integrity policy