San José State University
College of Engineering/Electrical Engineering
EE177, Digital System Interfacing

Section 01, Spring 2009

Instructor:	Tri Dinh
Office Location:	Engineering E383
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Email:	tri.q.dinh@gmail.com
Office Hours:	Half-hour before classes or by appointment
Class Days/Time:	TR 18:00 – 19:15
Classroom:	Engineering E329, Lab E244
Labroom:	Engineering E244 (Open Lab)
Prerequisites:	EE120

Course Description

This course covers hardware and software aspects of microcomputer interfacing specifications and organizations. The course includes topics in computer bus structures and specifications, hardware-software tradeoffs in digital system interfacing, data communication channels and bus interconnections, microcomputer peripheral interfacing, serial and parallel interfaces, A/D and D/A conversions, high speed system design.

Student Learning Objectives

Upon successful completion of this course, students will be able to:

1. Describe in reasonable details architect of a computer system.
2. Handle critical signals in a system: Clock, Power, Reset, etc…
3. Design a computer bus from given bus protocols and specifications
4. Hardware Design Memory Buses: EEPROM, SRAM, DRAM, DDR, etc…
5. Hardware Design Local Bus Standard: PCI, PCI-X, PCIe
6. Hardware Design I/O Bus Standard: UART, USB, GPIB.
7. Understand Data Acquisition & Design A/D or DAC circuit

8. Understand Signal Integrity Problems
9. Write a Test program to test external board via an USB port
10. Use CAD tools for design entry
11. Diag and debug a PCB
12. Design a PCB Hardware

Required Texts/Readings

Textbook

1. Thuy Le, "Digital System Interfacing, Lecture Notes," version 2.2, 2007
2. Thuy Le, "Digital System Interfacing, Lab Notes," version 2.0, 2007

Software Tools

ORCAD, MS Visual C++

Other Readings

1. Walter A. Triebel & Avtar Singh, "*The 8088 and 8086 Microprocessors*," Prentice Hall (any version)
2. Data sheets and Application Notes

Classroom Protocol

- Five laboratory exercises and a design projects will be assigned during the semester and are due by the due dates. All reports must be prepared neatly and professionally. The technical contents, format, completeness, and appearance of the report all contribute to the report's grade. Requests for rewriting the reports after they were graded are unacceptable.
- Student names on the reports must be your official names. Nicknames must not be used for the reports and exams.
- You are responsible to include all requested and necessary information in your reports. Reports must be condensed but completed, clear, firm, and prepared with care. Students can perform the experiment in groups but must turn-in their own individual reports. **Please keep in mind that reports will be graded for their technical contents, format, completeness, and appearance. Students may be asked to demo the experiments at any time.**

Dropping and Adding

Students are responsible for understanding the policies and procedures about add/drops, academic renewal, etc. Information on add/drops are available at http://info.sjsu.edu/web-dbgen/narr/soc-fall/rec-298.html. Information about late drop is available at http://www.sjsu.edu/sac/advising/latedrops/policy/ **.** Students should be aware of the current deadlines and penalties for adding and dropping classes.

Assignments and Grading Policy

Where the weights of all assignments and examinations are:

- Five Laboratory exercises and One projects: 40%
- One final project presentation 15%
- Midterm examination: 20%
- Final examination: 25%
- Scores above average curve B to A
- Average and below curve B- to F
- **Final project report must be submitted before the final exam date.**
- **There will be one midterm exam and a comprehensive final exam. The date of the midterm exam will be determined. The final exam date is Tuesday, May 19, 2009, 17:15-19:30**
- All exams will be CLOSE BOOK exams
- Exams will cover the assigned reading materials, discussed materials in the lectures, and information from the lab exercises and the design projects.
- There will be **no make-up** exams (in very special circumstances, written excuse and official proofs are required for making-up exam).
- To pass the course, a student must to take all exams and submit the final project.

University Policies

Academic integrity

Students should know that the University's Academic Integrity Policy is availabe at http://www.sa.sjsu.edu/download/judicial_affairs/Academic_Integrity_Policy_S07-2.pdf. Your own commitment to learning, as evidenced by your enrollment at San Jose State University and the University's integrity policy, require you to be honest in all your academic course work. Faculty members are required to report all infractions to the office of Student Conduct and Ethical Development. The website for Student Conduct and Ethical Development is available at http://www.sa.sjsu.edu/judicial_affairs/index.html.

Instances of academic dishonesty will not be tolerated. Cheating on exams or plagiarism (presenting the work of another as your own, or the use of another person's ideas without giving proper credit) will result in a failing grade and sanctions by the University. For this class, all assignments are to be completed by the individual student unless otherwise specified. If you would like to include in your assignment any material you have submitted, or plan to submit for another class, please note that SJSU's Academic Policy F06-1 requires approval of instructors.

Campus Policy in Compliance with the American Disabilities Act

If you need course adaptations or accommodations because of a disability, or if you need to make special arrangements in case the building must be evacuated, please make an appointment with me as soon as possible, or see me during office hours. Presidential Directive 97-03 requires that students with disabilities requesting accommodations must register with the DRC (Disability Resource Center) to establish a record of their disability

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Tentative Course Schedule

Week	Date	Topics
1	1/22	Introduction
2	1/27 1/29	Logic Design Review Signal & Bus Design
3	2/03 2/05	Signal & Bus Design Memory System Design
4	2/10 2/12	Error & Fault-Tolerant in Memory System, ECC PCI
5	2/17 2/19	PCI Bus Protocol Lab #1
6	2/24 2/26	PCI-X Lab #2
7	3/3 3/5	PCIe Overview PCIe Protocol
8	3/10 3/12	PCB Design Process Lab #3
9	3/17 3/19	Midterm Exam
10	3/24 3/26	Spring Break
11	3/31 4/2	Project Overview Project Start
12	4/7 4/9	Serial Interfacing:RS-232, UART Lab #4
13	4/14 4/16	USB USB Protocol
14	4/21 4/23	GPIB Lab#5
15	4/28 4/30	A/D DAC
16	5/5	Project Demo
Final Exam	5/19	**Final Exam (2 hours 15 minutes, comprehensive)**