San José State University
Engineering School/Electrical Engineering Department
EE227 Signal Integrity in AMS IC, Fall 2016

Instructor:	Denny Tang
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Office Hours:	Mon & Wed, 4:45-5:45pm
Class Days/Time:	Mon & Wed, 6-7:15pm
Classroom:	EE401
Prerequisites:	EE 221, familiar with Cadence Design System and Matlab/Simulink

Course Description

This course offers basics for students to learn the architect and the CMOS integrated circuitries of communication data channel. The main focus is the construction and realization of clock and data recovery (CDR) function. The vehicle is a wire-line data channel. Starting from high level functional concepts of a Phase Locked Loop (PLL), we will work our way down from system performance optimization to the choices of essential circuit blocks. System simulation and circuit simulation tools are used to optimize the PLL performance. Advanced CDR architect and data detection algorithm will also be covered.

Course Learning Outcomes (CLO) (Required)

CLO1. Understanding equalization concept in wire-line communication circuits
CLO2. Understanding phase locking techniques and clock and data recovery concepts
CLO3. Understanding performance metrics, such as Jitter tolerance, Jitter transfer, Jitter peaking, Random jitter, phase noise, BER and ….
CLO4. The ability to model equalizer, PLL and CDR using Matlab/Simulink
CLO5. The ability to design essential circuit block for data communication such as phase detector, charge pump, loop filter, ring and LC-tank voltage controlled oscillators, boosting filter, DC restoration
CLO6. Understanding mechanism and procedures for testing a phase locked loop

Required Texts/Readings

Textbook

1. *Instruction notes*
2. *"Design of Integrated Circuits for Optical Communications", B. Razavi, Wiley, 2012, ISBN-10-1118336941, ISBN-13: 978-1118336946*

Other Readings

"Phase-Locking in High Performance Systems from Device to Architectures". B. Razavi, IEEE Press. 2003

Course Requirements and Assignments

Class participation, assignments completion, midterm exam, design project and final exam

Grading Information (Required)

Examine will be closed book. However, students are allowed to bring ½ page of aid sheet, where can be option from this link (www.ardalan.ws/pdf). There will be no make-up exam and those absent will receive no credit. Students must write their answers clearly in an organized fashion. Further instructions will be provided during exams. The course is based on letter grading and grading percentage breakdown is as follow:

90% and above A
89%-85% A-
84%-82% B+
81%-79% B
78%-75% B
74%-72% B-
71%-69% C+
68%-65% C
64%-62% C-
61%-59% D+
58%-55% D
below 55% F

Total final grading is

Homework	10%
Class Q&A	5%
Mid-term Exam	30%
Design project	30%
Final Exam	25%

Classroom Protocol

Students are required to be in class on time and no cell phone conversation during the class.

University Policies

Per University Policy S16-9, university-wide policy information relevant to all courses, such as academic integrity, accommodations, etc. will be available on Office of Graduate and Undergraduate Programs' Syllabus Information web page at http://www.sjsu.edu/gup/syllabusinfo/"

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List the agenda for the semester including when and where the final exam will be held. Indicate the schedule is subject to change with fair notice and how the notice will be made available.

Course Schedule

Week	Date	Topics, Readings, Assignments, Deadlines
1	Aug-24 -16	Introduction to data channels

Week	Date	Topics, Readings, Assignments, Deadlines
1	Aug-29	Equalization and phase locking concept
2	Aug-31	Phase detector
2	Sept-5	Labor day
3	Sept-7	Current mode logic
3	Sept-12	Phase locked loop – system level
4	Sept-14	Phase locked loop – analog type 1
4	Sept-19	Phase locked loop – analog type 2
5	Sept-21	Nonlinear phase locking -1
5	Sept-26	Nonlinear phase locking -2 (CDR – clocked data recovery)
6	Sept-28	Phase detector modeling in Simulink
6	Oct-3	Clock, data source, and VCO modeling in Simulink
7	Oct-5	Linear PLL model in Simulink
7	Oct-10	Nonlinear PLL model in Simulink
8	Oct-12	Review
8	Oct-17	Mid-term
9	Oct-19	Performance Metrics -1
9	Oct-24	Performance Metrics -2
10	Oct-26	Introduction to Oscillators
10	Oct-31	Ring VCO, phase Noise in VCOs
11	Nov-2	LC Based VCO
11	Nov-7	Phase noise modeling in Simulink
12	Nov-9	Advanced CDR architectures 1 (Clock FWD, Embedded Clock)
12	Nov-14	Advanced CDR architectures 2 (Phase interpretation)
13	Nov-16	Advanced CDR architectures 3 (Lock injection)
13	Nov-21	Dual loop architectures
14	Nov-23	Digital PLL -1
14	Nov-28	Digital PLL -2
15	Nov-30	Analog equalization and DFE
15	Dec-5	Project demo
16	Dec-7	Project presentation 1 (=final exam)
Final Exam	Dec-12	Project presentation 2 (=final exam)