Electrical Engineering Department
San Jose State University

EE279 Special Topics in Digital Systems
VLSI Design-For-Testability
Fall 2007

Instructor: Dr. Rochit Rajsuman, Pinson Chair Professor
Office: 351
Office Hours: 2:45PM to 4:00PM
Class Time: MW 1330 – 1445
Class Room: TBD
Pre-Requisite: Instructor consent

Course Description
The objective of this course is to provide training so that students can work in industry as engineers who modify VLSI design for testability, engineers generally known as Design-for-Test engineers. Almost every chip contains design features for testability; these features facilitate wafer level testing as well as testing of the packaged ICs for structural and functional failures. After taking this course, a student should be able to work at a semiconductor design/manufacturing company.

Topics covered will include faults in digital and analog circuits; stuck-at, bridging, open, functional fault models, test generation methods for digital logic, analog, memories and microprocessors, scan design to enhance testability of digital logic, boundary scan design, analog boundary scan, built-in self-test for digital logic, design-for-testability of mixed-signal circuits, data converters (DAC/ADC), frequency synthesizers (PLL/DLL), testability features of ROM, SRAM, DRAM and Flash, built-in self-test in memory, microprocessor's functional testing, concepts of built-in self-repair.

Text Book: Rochit Rajsuman, Digital Hardware Testing, Artech House

Reference Books:
1. Rochit Rajsuman, System-on-a-chip: Design and Testing, Artech House
2. Alex Miczo, Digital logic testing and simulation, John Wiley
3. Abromovici, Breuer and Friedman, Digital system testing and testable design.

Grading

Homework: 30%	A: 90 or above
Mid-term Exam: 30%	B: 80 to 90
Final Exam: 40%	C: 70 to 80
	D: 60 to 70

Lectures

1. Introduction: Necessity and cost of testing, faults, failures and errors.
2. Faults in digital circuits, fault models, line stuck-at model, transistor level fault models, fault equivalence and dominance.
3. Test generation for digital circuits, path sensitization, Boolean difference
4. Test generation algorithms, test generation tools by Synopsys, Mentor Graphics and Cadence.
5. Testing of PLAs, fault models, test generation, design features in PLAs for test.
6. Error detection and correction in data path.
7. Testing of state machines.
8. Scan and level sensitive scan designs for digital logic and state machines
9. Boundary scan design, IEEE 1149.1 standard
10. Random/pseudo random tests, LFSR and MISR circuit designs, test synthesis tools by Synopsys, Mentor Graphics and Cadence
11. Built-in self-test, scan based built-in self-test,
12. Signature analysis, compression and aliasing
13. Analog and mixed signal fault models, specification based testing
14. Analog boundary scan, IEEE 1149.4 standard
15. Testing of amplifiers and switched capacitor filters
16. Testing of ADC and DAC, audio and video DACs, analog built-in self-test.
17. Testing of PLLs
18. Memory fault models, algorithms to generate memory tests,
19. Design features in memories for test
20. Built-in self-test in memories, memory built-in self-test tools by Synopsys, Mentor Graphics and Cadence.
21. Redundancy and built-in self-repair in memories.
22. Microprocessor test, functional tests of hardwired control and micro-programmed control.
23. Examples of microprocessor's test features, ARM processor, Pentium, SPARC
24. Current based testing, Iddq, current signature
25. Test standards for core based design, IEEE 1500.