Electrical Engineering Department
San Jose State University

High Speed CMOS Circuits (EE224)
Fall 2007

Instructor: Dr. Rochit Rajsuman, Pinson Chair Professor
Office: 351
Office Hours: T R 6:30PM to 7:30PM and by appointment
Class Time: T R 1930 – 2045
Class Room: 336
Pre-Requisite: EE166 and EE221

Course Description
Analysis and design of digital integrated circuits, static and dynamic CMOS logic gates, Programmable and Cell based design, Memories, I/Os. Speed, power and area considerations, floor plan, clock and power distribution at the chip level.
Students will become familiar with the designs of following circuits:

1. Design of simple and complex logic gate, decoders, multiplexers, flip-flops and registers, counters, register files, adders, ALUs, multipliers, SRAM, DRAM, FLASH and EEPROM memories, FIFO and CAM memories, simple and high-load driving I/Os. Layout styles of these circuits and technology scaling principles.
2. Different forms of implementation of above circuits including static and dynamic circuit styles. Domino CMOS, Clocked CMOS, CVSL, Zipper and NORA dynamic circuit implementations.
3. Implementation for higher speed. Extensive analyses for improving switching speed and higher data rate.
4. Implementation for lower power.
5. Clock generation and distribution circuits.
6. Power distribution methods at the chip level.

Project: Course requires a class project of complete design of a high-speed circuit. Students are expected to make layout, schematics and simulations to demonstrate the fully functional circuit block.

Text Book: Neil Weste and David Harris, CMOS VLSI Design
Reference Books

1. Michael Smith, Application Specific Integrated Circuits
2. Wayne Wolf, Modern VLSI Design
3. John Uyemura, CMOS Logic Circuit Design

Grading

Homework: 25%	A: 90 or above
Project: 25%	B: 80 to 90
Mid-term Exam: 25%	C: 70 to 80
Final Exam: 25%	D: 60 to 70

Lectures

1. Introduction, semiconductor energy band, effect of doping, mobility of charge carriers, p-n junction, p-n-p junction, MOSFET, NMOS and PMOS.
2. Detailed MOSFET operation, effect of substrate bias, impact on threshold voltage, channel length modulation, MOSFET modeling.
3. CMOS Inverter, DC and transient characteristics, transistor sizing, effect of β_n/β_p, noise margins, latch-up.
4. CMOS logic gates, NAND, NOR, CMOS pass transistor logic.
5. CMOS Circuit Manufacturing, general process steps, masks making.
6. CMOS circuit layouts, stick diagrams, layout design styles, cell design, resistors, capacitors, inductors.
7. CMOS complex gates, half and full adders, half and full subtractor.
8. Circuit performance, resistance estimation, capacitance estimation, delay using RC model, transmission line, transistor chain.
9. Inverter rise and fall time, switching delay, NAND, NOR and complex Gate delay, methods to improve Gate delay.
10. Power consumption, static and dynamic power, power-delay product, miller effect.
11. Ring oscillator, process monitor.
12. Constant electric field and constant voltage scaling, impact of scaling on transistor and transmission line.
13. CMOS Gate design styles, transistor optimization.
14. Static combinational logic circuits.
15. Dynamic combinational logic, domino, clocked CMOS, CVSL and NORA logic.
16. Clocking styles, 2 and 4 phase clocking, clock design.
17. Latches and flip-flops, high speed registers and counters.
18. CMOS memories, ROM, SRAM, DRAM, Flash
19. I/O design, design of I/O buffers.
20. Data buses, methods to drive large load.
21. High-speed sub-circuit design, decoders, multiplexers, carry look-ahead and fast adder.
22. Parallel multipliers, divider, register files, FIFO and CAM.
23. State machine design
24. Power and thermal considerations in high-speed circuits, speed and power optimization.