Course Title: Digital Design Using VHDL

Meeting: Section 1: T Th 19:00 -19:50, Clark 229

Instructor:  
  Dr. Tri Caohuu, ENG 375  
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Course Outline:  
This course presents a comprehensive approach to HDL-based digital design methodology using VHDL. Students will learn the basic structures of VHDL, VHDL simulation and synthesis. Selected topics on performance level simulation and synthesis will also be discussed.  
The students are required to do exercises and a design project in the accompanied Laboratory. The course is intended for senior students with background in logic design and computer organization.

Text books:  
1. VHDL Design, Representation and Synthesis  
2. Notes and Handouts

Reference:  
VHDL Primer by J. Bhasker,  
Prentice Hall, 1999

Grading policy:  
  Homework and Quizzes 10%  
  Midterm 25%  
  Laboratory 30%  
  Final Exam 35%

Office Hour:  
W: 15:00 - 16:30 ; Friday 10:30 – 12:00  
ENGR375

Open Laboratory:  
E 291/Unix-based and EE 389/PC-based
COURSE OUTLINE

I. Introduction        Notes, Chap. 1&2
II. Basic Constructs of VHDL     Chapter 3
III. VHDL Parallelism and its Simulation Kernel  Chap. 4
IV. Modeling Techniques     Notes
V. Chip Level Modeling     Chap. 5,6
VI. System Level Modeling     Chap. 8
VII. ASIC/FPGA Design Process     Chap. 9
VIII. Modeling for Synthesis     Chap. 10
IX. Design Project  Design Spec.

PLEASE DO NOT CONSUME FOOD IN THE CLASSROOM

EE@SJSU
Honesty and Respect for Others and Public Property

EE HONOR CODE
The Electrical Engineering Department will enforce the following Honor Code that must be read and accepted by all students.

“I have read the Honor Code and agree with its provisions. My continued enrollment in this course constitutes full acceptance of this code. I will NOT:

• Take an exam in place of someone else, or have someone take an exam in my place
• Give information or receive information from another person during an exam
• Use more reference material during an exam than is allowed by the instructor
• Obtain a copy of an exam prior to the time it is given
• Alter an exam after it has been graded and then return it to the instructor for re-grading
• Leave the exam room without returning the exam to the instructor.”

Measures Dealing with Occurrences of Cheating

Department policy mandates that the student or students involved in cheating will receive an “F” on that evaluation instrument (paper, exam, project, homework, etc.) and will be reported to the Department and the University.

A student’s second offense in any course will result in a Department recommendation of suspension from the University.

EE/CE 179 HONOR CODE

In addition to EE Honor Code, EE/CE 179 students understand that professional attitude is necessary to maintain a comfortable academic environment. For examples:

- I do not just skip the lecture and then ask the instructor to summarize the lecture for me later on. Office hours are for students to have questions, not for the instructor to summarize the lecture for any specific student.
- I come to the class on time and leave the class at the end of the lecture.
- To minimize possible tension during the exams, I WILL follow the exam rules closely.
- I work on the lab assignments and final project by myself.
- I understand that long-term learning is my responsibility and so I always keep it up

I strongly believe that NOT any statement similarly to examples below can be used:

- I am working full-time and so do not have enough time for the class.
- I have quite many classes this semester and so I do not have enough time for the class.
- I just need a passing grade to graduate this semester.
- I live far away from the campus and so I can not come to the class often.
- etc., etc.,