San José State University Department of
Electrical Engineering
EE98, Introduction to Circuit Analysis, Section 4, Spring 2020

Instructor: Sotoudeh Hamedi-Hagh

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Email: sotoudeh.hamedi-hagh@sjsu.edu

Office Hours: Tu 10:15AM-10:30AM, 11:45AM-1:00PM or with Appointment

Class Days/Time: TuTh 10:30AM-11:45AM

Classroom: ENGR301

Prerequisites: ENGR 10 and PHYS 51 with a C or better. Co-Requirement Mat 133A

Course Web Page: See SJSU Canvas Website

Course Description
Circuit laws and nomenclature, resistive circuits with DC sources, ideal operational amplifier, controlled sources, natural and complete response of simple circuits, steady-state sinusoidal analysis and power calculations.

Course Goals and Student Learning Objectives
The objective of this course is to introduce the basics of AC/DC and transient analysis. This course builds on the foundations of physics and mathematics and is essential for all upper division EE courses.

Topics Covered:
- Ohm’s law and Kirchhoff’s laws
- Series and parallel circuits
- Superposition
- Thevenin and Norton Equivalent
- Maximum power transfer
- Nodal and mesh analysis
- Active and op amp circuits
- Capacitors and inductors
- Transient analysis
- Steady state analysis
- AC power
Course Content Learning Objectives:
Upon successful completion of this course, students will be able to:

1. Determine voltages and currents in a DC circuit consisting of resistors, current sources, voltage sources, and dependent sources.
2. Determine Thevenin and Norton equivalent circuit of a DC circuit and find the maximum power output of a DC circuit.
3. Determine the DC gain and operating point of an OP amp circuit.
4. Determine the transient response of a first and second order circuit consisting of RLC.
5. Determine the sinusoidal steady state response of a circuit consisting of RLC.
6. Determine the power delivered and absorbed by an element in a RLC circuit.

The following table shows the level of this course’s contribution to the achievement of EE program outcomes and meeting the ABET program requirements. Bloom’s Taxonomy is used in the definition of learning level: 0-Not Applicable, 1-knowledge, 2-Comprehension, 3-Application, 4-Analysis, 5-Synthesis, 6-Evaluation.

ABET Student outcomes:

1. An ability to identify, formulate, and solve complex engineering problems by applying principles of engineering, science, and mathematics (3)
2. An ability to apply engineering design to produce solutions that meet specified needs with consideration of public health, safety, and welfare, as well as global, cultural, social, environmental, and economic factors (0)
3. An ability to communicate effectively with a range of audiences (3)
4. An ability to recognize ethical and professional responsibilities in engineering situations and make informed judgments, which must consider the impact of engineering solutions in global, economic, environmental, and societal contexts (0)
5. An ability to function effectively on a team whose members together provide leadership, create a collaborative and inclusive environment, establish goals, plan tasks, and meet objectives (0)
6. An ability to develop and conduct appropriate experimentation, analyze and interpret data, and use engineering judgment to draw conclusions (0)
7. An ability to acquire and apply new knowledge as needed, using appropriate learning strategies. (0)

Texts/Readings


Dropping, Adding and Staying:

Students are responsible for understanding the policies and procedures about add/drop, grade forgiveness, etc. Refer to the current semester’s Catalog Policies section at http://info.sjsu.edu/static/catalog/policies.html. Add/drop deadlines can be found on the current academic calendar web page located at
http://www.sjsu.edu/academic_programs/calendars/academic_calendar/. The Late Drop Policy is available at http://www.sjsu.edu/aars/policies/latedrops/policy/. Students should be aware of the current deadlines and penalties for dropping classes.

There are practice assignments (No credit) in canvas to make sure you will do well in the class. Although these assignments have due dates and have symbolic grades, students can keep doing them until they achieve the required results. There is no penalty for retrying an assignment. For the full policy and explanation please see the Add /Drop /Stay policy in the canvas shell.

**Homework**

Assignments might be managed though the Canvas.

**Exams**

There will be two midterm examinations, and a final exam. All exams will be closed-book. For midterms and the final exam, a calculator) is allowed. The formula sheet will be provided to you within your exam. A photographic ID will be required. Unless there is a legal, serious documentation for missing an exam, make-up exams are not allowed.

**Grading Policy**

The following weighting will be used in calculating the overall course grades.

- Project assignments: 20%
- Quizzes: 3×5%
- Midterm #1: 15%
- Midterm #2: 15%
- Final Exam: 35%
  - 94% and above A
  - 93% - 90% A-
  - 89% - 87% B+
  - 86% - 84% B
  - 83% - 80% B-
  - 79% - 77% C+
  - 76% - 74% C
  - 73% - 70% C-
  - 69% - 67% D+
  - 66% - 64% D
  - 63% - 60% D-
  - below 60% F

**Academic integrity**

Your commitment as a student to learning is evidenced by your enrollment at San Jose State University. The University’s Academic Integrity policy, located at http://www.sjsu.edu/senate/S07-2.htm, requires you to be honest in all your academic
course work. Faculty members are required to report all infractions to the office of Student Conduct and Ethical Development. The Student Conduct and Ethical Development website is available at http://dev.sjsu.edu/studentconduct/.

Instances of academic dishonesty will not be tolerated. Cheating on exams or plagiarism (presenting the work of another as your own, or the use of another person’s ideas without giving proper credit) will result in a failing grade and sanctions by the University. For this class, all assignments are to be completed by the individual student unless otherwise specified. If you would like to include your assignment or any material you have submitted, or plan to submit for another class, please note that SJSU’s Academic Policy S07-2 requires approval of instructors.

Campus Policy in Compliance with the American Disabilities Act

If you need course adaptations or accommodations because of a disability, or if you need to make special arrangements in case the building must be evacuated, please make an appointment with me as soon as possible, or see me during office hours. Presidential Directive 97-03 requires that students with disabilities requesting accommodations must register with the Disability Resource Center (DRC) at http://www.drc.sjsu.edu/ to establish a record of their disability.

EE Department Honor Code

The Electrical Engineering Department will enforce the following Honor Code that must be read and accepted by all students.

I have read the Honor Code and agree with its provisions. My continued enrollment in this course constitutes full acceptance of this code. I will NOT:

• Take an exam in place of someone else, or have someone take an exam in my place
• Give information or receive information from another person during an exam
• Use more reference material during an exam than is allowed by the instructor
• Obtain a copy of an exam prior to the time it is given
• Alter an exam after it has been graded and then return it to the instructor for re-grading
• Leave the exam room without returning the exam to the instructor.”
• Department policy mandates that the student or students involved in cheating will receive an “F” on that evaluation instrument (paper, exam, project, homework, etc.) and will be reported to the Department and the University.
• A student’s second offense in any course will result in a Department recommendation of suspension from the University.
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<td>Introduction</td>
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<td>9.1 Introduction 9.2 Sinusoids, 9.3 Phasor</td>
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<td>Review (Quiz #1)</td>
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<td>3.2 Nodal analysis, 3.3 Nodal analysis with voltage sources</td>
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<td>5.1 Non-ideal amplifier 5.2 Ideal amplifier</td>
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<td>5.8 Cascade Opamp circuit</td>
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<td>7.2 Source free RC circuit, 7.3 Source free RL circuit</td>
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<td>7.6 Step response of an RC &amp;RL circuit, 8.2 initial and final values</td>
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