San José State University
Department of Electrical Engineering
EE 98, Introduction to Circuit Analysis, Section 3, Spring 2019

Instructor: Eveline Bellegarda
Office Location: ENGR 383
Telephone: (408)924 3950
Email: Eveline.Bellegarda@sjsu.edu
Office Hours: After Class 1:30PM – 2:30PM or with Appointment
Class Days/Time: MoWe 12:00PM - 1:15PM
Classroom: Engineering Building 345
Prerequisites: PHYS 51 with a C or better.
Co-Req Mat 133A
Course Web Page: See SJSU Canvas Website

Course Description
Circuit laws and nomenclature, resistive circuits with DC sources, ideal operational
amplifier, controlled sources, natural and complete response of simple circuits,
steady-state sinusoidal analysis and power calculations.

Course Goals and Student Learning Objectives
The objective of this course is to introduce the basics of AC/DC and transient
analysis. This course builds on the foundations of physics and mathematics and is
essential for all upper division EE courses.

Topics Covered:
- Ohm’s law and Kirchhoff’s laws
- Series and parallel circuits
- Superposition
- Thevenin and Norton Equivalent
- Maximum power transfer
- Nodal and mesh analysis
- Active and op amp circuits
Course Content Learning Objectives:

Upon successful completion of this course, students will be able to:

1. Determine voltages and currents in a DC circuit consisting of resistors, current sources, voltage sources, and dependent sources.
2. Determine Thevenin and Norton equivalent circuit of a DC circuit and find the maximum power output of a DC circuit.
3. Determine the DC gain and operating point of an OP amp circuit.
4. Determine the transient response of a first and second order circuit consisting of RLC.
5. Determine the sinusoidal steady state response of a circuit consisting of RLC.
6. Determine the power delivered and absorbed by an element in a RLC circuit.
7. Document a simple circuit project
8. Plan the layout and solder a simpler circuit project
9. Test a simple circuit and analyze collected data

The following table shows the level of this course’s contribution to the achievement of EE program outcomes and meeting the ABET program requirements. Bloom’s Taxonomy is used in the definition of learning level: 0-Not Applicable, 1-knowledge, 2-Comprehension, 3-Application, 4-Analysis, 5-Synthesis, 6-Evaluation.

ABET Student outcomes:

1. an ability to identify, formulate, and solve complex engineering problems by applying principles of engineering, science, and mathematics 3
2. an ability to apply engineering design to produce solutions that meet specified needs with consideration of public health, safety, and welfare, as well as global, cultural, social, environmental, and economic factors 0
3. an ability to communicate effectively with a range of audiences 3
4. an ability to recognize ethical and professional responsibilities in engineering situations and make informed judgments, which must consider the impact of engineering solutions in global, economic, environmental, and societal contexts 0
5. an ability to function effectively on a team whose members together provide leadership, create a collaborative and inclusive environment, establish goals, plan tasks, and meet objectives 0
6. an ability to develop and conduct appropriate experimentation, analyze and interpret data, and use engineering judgment to draw conclusions 0
7. an ability to acquire and apply new knowledge as needed, using appropriate learning strategies. 0
Texts/Readings


Dropping, Adding and Staying:

Students are responsible for understanding the policies and procedures about add/drop, grade forgiveness, etc. Refer to the current semester’s Catalog Policies section at http://info.sjsu.edu/static/catalog/policies.html. Add/drop deadlines can be found on the current academic calendar web page located at http://www.sjsu.edu/academic_programs/calendars/academic_calendar/. The Late Drop Policy is available at http://www.sjsu.edu/aars/policies/latedrops/policy/. Students should be aware of the current deadlines and penalties for dropping classes.

Directed Self Placement (Add/Drop/Stay Procedure):
This course uses Gateway assignments to make sure you will do well in the class. Students will be encouraged to drop if they do not maintain a 90% average grade in the HW up to the last day to add. You will be notified you are not meeting the standard via your sjsu.edu email. If you do not respond to the email you will be dropped from the course. These assignments that are checked are HW 1-6, but a warning will be sent via your sjsu.edu email around the due date of HW4. Although the automatically graded assignments have due dates, students can keep doing them until they achieve the required results. There is no penalty for re-trying an assignment. For the full policy, please see the Directed Self Placement (Add/Drop/Stay Procedure) in the canvas shell.

Homework
All assignments are managed though the Canvas.

Exams
There will be two midterm examinations, and a final exam. All exams will be closed-book. For midterms and the final exam, a calculator) is allowed. An equation sheet will be provided for you. A photographic ID will be required. Unless there is a documented, serious explanation for missing an exam, make-up exams will not be allowed.

Grading Policy
The following weighting will be used in calculating the overall course grades.

- Project: 10%
- Homework: 15%
  - All HW is submitted and graded in the canvas shell.
  - The Automatically graded online HW can be done as many times as you like, and does not close, although they have due dates.
  - The Human graded HW is graded once, but depending on instructor resources may be re-submitted.
- Midterm #1: 25%
- Midterm #2: 25%
- Final Exam: 25%
- 94% and above A
- 93% - 90%  A-
- 89% - 87%  B+
- 86% - 84%  B
- 83% - 80%  B-
- 79% - 77%  C+
- 76% - 74%  C
- 73% - 70%  C-
- 69% - 67%  D+
- 66% - 64%  D
- 63% - 60%  D-
- below 60%  F

There will be no make ups given for midterms. If you miss a midterm for any reason, you can make up the grade on the final exam. If you have three finals on the same day, you can take the final on the final exam make up day posted in the university calendar.

Academic integrity
Your commitment as a student to learning is evidenced by your enrollment at San Jose State University. The University’s Academic Integrity policy, located at http://www.sjsu.edu/senate/S07-2.htm, requires you to be honest in all your academic course work. Faculty members are required to report all infractions to the office of Student Conduct and Ethical Development. The Student Conduct and Ethical Development website is available at http://dev.sjsu.edu/studentconduct/.

Instances of academic dishonesty will not be tolerated. Cheating on exams or plagiarism (presenting the work of another as your own, or the use of another person’s ideas without giving proper credit) will result in a failing grade and sanctions by the University. For this class, all assignments are to be completed by the individual student unless otherwise specified. If you would like to include your assignment or any material you have submitted, or plan to submit for another class, please note that SJSU’s Academic Policy S07-2 requires approval of instructors.

Campus Policy in Compliance with the American Disabilities Act
If you need course adaptations or accommodations because of a disability, or if you need to make special arrangements in case the building must be evacuated, please make an appointment with me as soon as possible, or see me during office hours. Presidential Directive 97-03 requires that students with disabilities requesting accommodations must register with the Disability Resource Center (DRC) at http://www.drc.sjsu.edu/ to establish a record of their disability.

EE Department Honor Code
The Electrical Engineering Department will enforce the following Honor Code that must be read and accepted by all students. 

I have read the Honor Code and agree with its provisions. My continued enrollment in this course constitutes full acceptance of this code. I will NOT:

• Take an exam in place of someone else, or have someone take an exam in my place
• Give information or receive information from another person during an exam
• Use more reference material during an exam than is allowed by the instructor
• Obtain a copy of an exam prior to the time it is given
• Alter an exam after it has been graded and then return it to the instructor for re-grading
• Leave the exam room without returning the exam to the instructor.”
• Department policy mandates that the student or students involved in cheating will receive an “F” on that evaluation instrument (paper, exam, project, homework, etc.) and will be reported to the Department and the University.
• A student’s second offense in any course will result in a Department recommendation of suspension from the University.

---

**EE98, Introduction to Circuit Analysis**

<table>
<thead>
<tr>
<th>Module</th>
<th>Date</th>
<th>Topic/Readings</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1/28/2019</td>
<td>9.1 Introduction 9.2 Sinusoids, 9.3 Phasor</td>
</tr>
<tr>
<td>2</td>
<td>1/30/2019</td>
<td>9.4 Phasor relationships for circuit elements, 9.5 Impedance and admittance, 9.7 Impedance combinations</td>
</tr>
<tr>
<td>3</td>
<td>2/4/2019</td>
<td>11.2 Instantaneous and average Power, 11.4 Effective or rms value, 11.5 Apparent power and power factor</td>
</tr>
<tr>
<td>4</td>
<td>2/6/2019</td>
<td>Learn LTspice,</td>
</tr>
<tr>
<td>5</td>
<td>2/11/2019</td>
<td>4.2 Linearity, bias an LED, Power Supply, Dependent source</td>
</tr>
<tr>
<td>6</td>
<td>2/13/2019</td>
<td>4.3 Superposition, Transistor</td>
</tr>
<tr>
<td>7</td>
<td>2/18/2019</td>
<td>4.4 Source transformation, 4.5 Thevenin theorem</td>
</tr>
<tr>
<td>8</td>
<td>2/20/2019</td>
<td>4.6 Norton theorem, 4.7 Maximum power transfer</td>
</tr>
<tr>
<td>9</td>
<td>2/25/2019</td>
<td>Review</td>
</tr>
<tr>
<td>10</td>
<td>2/27/2019</td>
<td>Midterm 1 (Show all work for full credit.)</td>
</tr>
<tr>
<td>11</td>
<td>3/4/2019</td>
<td>3.2 Nodal analysis, 3.3 Nodal analysis with voltage sources</td>
</tr>
<tr>
<td>12</td>
<td>3/6/2019</td>
<td>3.4 Mesh analysis,</td>
</tr>
<tr>
<td>13</td>
<td>3/11/2019</td>
<td>5.1 Non-ideal amplifier 5.2 Ideal amplifier</td>
</tr>
<tr>
<td>14</td>
<td>3/13/2019</td>
<td>5.6 Summing amplifier, 5.7 Difference amplifier</td>
</tr>
<tr>
<td></td>
<td>Date</td>
<td>Topic</td>
</tr>
<tr>
<td>----</td>
<td>------------</td>
<td>-------------------------------------------------</td>
</tr>
<tr>
<td>15</td>
<td>3/18/2019</td>
<td>5.8 Cascade op amp circuit</td>
</tr>
<tr>
<td>16</td>
<td>3/20/2019</td>
<td>OPAMP Applications</td>
</tr>
<tr>
<td>17</td>
<td>3/25/2019</td>
<td>Board Layout</td>
</tr>
<tr>
<td>18</td>
<td>3/27/2019</td>
<td>Project</td>
</tr>
<tr>
<td></td>
<td>4/1/2019</td>
<td>Class does not meet. Campus is closed.</td>
</tr>
<tr>
<td></td>
<td>4/3/2019</td>
<td>Class does not meet. Campus is closed.</td>
</tr>
<tr>
<td>19</td>
<td>4/8/2019</td>
<td>Simple Filters, Bode plots</td>
</tr>
<tr>
<td>20</td>
<td>4/10/2019</td>
<td>Review</td>
</tr>
<tr>
<td>21</td>
<td>4/15/2019</td>
<td>Midterm 2 (Show all work for full credit.)</td>
</tr>
<tr>
<td>22</td>
<td>4/17/2019</td>
<td>7.2 Source free RC circuit, 7.3 Source free RL circuit</td>
</tr>
<tr>
<td>23</td>
<td>4/22/2019</td>
<td>7.6 Step response of an RC &amp; RL circuit</td>
</tr>
<tr>
<td>24</td>
<td>4/24/2019</td>
<td>8.2 Finding initial and final values</td>
</tr>
<tr>
<td>26</td>
<td>5/1/2019</td>
<td>8.5/8.6 Step series parallel RLC circuit</td>
</tr>
<tr>
<td>27</td>
<td>5/6/2019</td>
<td>Project</td>
</tr>
<tr>
<td>28</td>
<td>5/8/2019</td>
<td>8.7/8.8 General Second Order OPAMP</td>
</tr>
<tr>
<td>29</td>
<td>5/13/2019</td>
<td>Review Semester</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Final Exam</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Friday, May 17, 0945-1200, Classroom</td>
</tr>
</tbody>
</table>