

San José State University
Electrical Engineering Department
EE287, CMOS ASIC Design, Spring 2018

Course and Contact Information

Instructor:	Morris Jones
Office Location:	E295 (It's a lab, knock)
Telephone:	408-507-4698 (Cell)
Email:	morris.jones@sjsu.edu
Office Hours:	T&Th 4:30-5:30 PM (F by appointment)
Class Days/Time:	Tu&Th 7:30-8:45PM
Classroom:	E341
Prerequisites:	EE270 or EE271. (Students should be able to create Verilog designs before taking EE287)

Faculty Web Page and MYSJSU Messaging

Course materials such as syllabus, handouts, notes, assignment instructions, etc. can be found on the Canvas learning management system course website. You are responsible for regularly checking with the messaging system through MySJSU/Canvas to learn of any updates.

Course Description

EE287 is an overview of CMOS ASIC concepts and design. Industry tools will be used to illustrate principles taught. Overall concepts will be tied together by a design project. Project team work will be stressed.

Course Learning Outcomes (CLO)

1. Practice and demonstrate critical thinking
2. Understand requirements and translate them to a high level design language
3. Understand capabilities and limitations of CMOS logic and adjust designs to best use CMOS ASIC technologies.
4. Demonstrate common ASIC team rules, and articulate the purposes for such rules.
5. Demonstrate an ability to use industry synthesis tools to achieve desired project objectives.
6. Demonstrate an understanding of module interfaces, pipe lining, design for test, test pattern generation, and BIST.
7. Modify designs to achieve performance objectives.
8. Perform an ASIC design from requirements to timing verification

Course goals and objectives

1. Prepare students to be productive members of an industrial ASIC design team

2. Prepare students for graduate projects involving digital circuits using ASIC techniques and synthesis
3. Provide an understanding of the ASIC life cycle
4. Provide an opportunity developing teamwork skills
5. Provide an environment where students learn to think critically
6. Provide an environment where students learn to enjoy the learning and designing process

Required Texts/Readings

Textbook

There is no text book. The class is taught from notes, and industrial materials. All notes are on the Canvas website at sjsu.instructure.com

Login using your SJSUone ID, and your SJSUone password.

Other Readings

Data sheets and other materials may be found on the CANVAS website under the modules section.

Other equipment / material requirements

Students will be required to complete lab assignments, and have access to the E289 and E291 labs. These machines have industrial logic design tools. You can get an access code for the labs from the EE office. A limited number of machines are remotely accessible through VNC. Access eecad.engr.sjsu.edu through VNC.

Course Requirements and Assignments

The following describes the course requirements and assignments. The details of each assignment are on the Canvas system. Detailed schedule information is at the document end.

Homework (10%): Homework will consist of a mix of analysis and design problems. Analytical and CAD based techniques will be required to solve problems. The homework is designed to reinforce lecture concepts and prepare the student for the exams and class project. Homework assignments will be due according to the green sheet. In addition to homework, online and in class assessments (quizzes) are included in the homework scores. Each student needs to solve the homework problems individually.. Copied homework will receive a score of zero. Both the source and destination students will receive the zero score. Online assessments (quizzes) must be completed individually.

- a. All homework shall be submitted on the Canvas system.
 - i. You can scan paper documents at the academic success center
 - ii. No homework is accepted in class, by email, canvas message attachments, or under the office door
 1. You are expected to do your own homework
 2. Developing professional discipline through on time homework submission is expected and required. The Canvas system will not inform you an assignment is due or late. Homework may not be submitted when the assignment closes on Canvas. Homework must be submitted through the electronic system.

Project (15%): The project is a design problem. The specifications will be found on canvas. Teams of 2-3 people are expected to work on the design problem. The project will not be accepted late. A maximum of 50% of the score can be earned if the design does not pass the test bench (All code present, but not debugged). To discourage *borrowing* of other teams efforts, the designs will be run through a recursive difference engine, and the score will be reduced to zero if similar in any significant way to other submitted designs. Both teams will be penalized. The instructor will not attempt to determine which design was copied. Don't share project designs.

Midterm (35%): Covers the first half of the semester. A study guide is available on the web site with typical questions. Several past midterms are also posted on the web. All EE287 exams are closed book, no notes. Scratch paper will be provided during the exam. You will be seated randomly in the class, and there will be multiple versions of the exam. (2-5 typically). You should bring a calculator and writing instruments to the exam. Programmable calculators are not allowed

unless completely cleared. Cell phones may not be used in exams. Each exam version is normalized to the high score on that version to provide fairness. Photo ID is required when you turn in your exam.

Final Exam (40%): The final exam will be the same format as the midterm except it will cover the entire semester with emphasis on the last half of the semester. All EE287 exams are closed book, no notes. Scratch paper will be provided during the exam. You will be seated randomly in the class, and there will be multiple versions of the exam. (2-5 typically). You should bring a calculator and writing instruments to the exam. The rules are the same as the midterm. Photo ID is required when you turn in your exam.

The CLO's are shown in practice by the following activities. They are tested on the midterm and the final to measure and ensure understanding.

Activity	CLO
Project	1,2,3,4,5,8
Design HW2	4,5,6,7
Paper 1	3

NOTE that [University policy F69-24](http://www.sjsu.edu/senate/docs/F69-24.pdf) at <http://www.sjsu.edu/senate/docs/F69-24.pdf> states that “Students should attend all meetings of their classes, not only because they are responsible for material discussed therein, but because active participation is frequently essential to insure maximum benefit for all members of the class. Attendance per se shall not be used as a criterion for grading.”

Grading Policy

Grade	%	Comment
A	100%	May vary down from 100%
A-	90 – 99.9999%	May vary down from 99.9999%
B+	88-89.9999%	
B	84-87.9999%	
B-	80-83.9999%	
C+	78-79.99999%	No C or C- grades may be given in EE287. If below 78%, expect an F.
F	0-77.99999%	

The +/- grade breaks are set by adjusting the thresholds up and down to meet the department grade distribution guidelines. The break points will not be known until the semester is over, and the class composite scores are available. In past semesters, the A- typically breaks at 97%, the B+ breaks at 88%, and the F break has varied between 75 to 78%. The breaks will be no higher than those shown.

Note that “All students have the right, within a reasonable time, to know their academic scores, to review their grade-dependent work, and to be provided with explanations for the determination of their course grades.” See

[University Policy F13-1](http://www.sjsu.edu/senate/docs/F13-1.pdf) at <http://www.sjsu.edu/senate/docs/F13-1.pdf> for more details. All grading information is available real time on the Canvas system.

Classroom Protocol

Students will turn their cell phones off or put them on vibrate mode while in class. They will not answer their phones in class. Students whose phones disrupt the course and do not stop when requested by the instructor will be referred to the Judicial Affairs Officer of the University.

University Policies

General Expectations, Rights and Responsibilities of the Student

As members of the academic community, students accept both the rights and responsibilities incumbent upon all members of the institution. Students are encouraged to familiarize themselves with SJSU's policies and practices pertaining to the procedures to follow if and when questions or concerns about a class arises. See [University Policy S90-5](http://www.sjsu.edu/senate/docs/S90-5.pdf) at <http://www.sjsu.edu/senate/docs/S90-5.pdf>. More detailed information on a variety of related topics is available in the [SJSU catalog](http://info.sjsu.edu/web-dbgen/narr/catalog/rec-12234.12506.html), at <http://info.sjsu.edu/web-dbgen/narr/catalog/rec-12234.12506.html>. In general, it is recommended that students begin by seeking clarification or discussing concerns with their instructor. If such conversation is not possible, or if it does not serve to address the issue, it is recommended that the student contact the Department Chair as a next step.

Dropping and Adding

Students are responsible for understanding the policies and procedures about add/drop, grade forgiveness, etc. Refer to the current semester's [Catalog Policies](http://info.sjsu.edu/static/catalog/policies.html) section at <http://info.sjsu.edu/static/catalog/policies.html>. Add/drop deadlines can be found on the current academic year calendars document on the [Academic Calendars webpage](http://www.sjsu.edu/provost/services/academic_calendars/) at http://www.sjsu.edu/provost/services/academic_calendars/. The [Late Drop Policy](http://www.sjsu.edu/aars/policies/latedrops/policy/) is available at <http://www.sjsu.edu/aars/policies/latedrops/policy/>. Students should be aware of the current deadlines and penalties for dropping classes.

Information about the latest changes and news is available at the [Advising Hub](http://www.sjsu.edu/advising/) at <http://www.sjsu.edu/advising/>.

Consent for Recording of Class and Public Sharing of Instructor Material

[University Policy S12-7](http://www.sjsu.edu/senate/docs/S12-7.pdf), <http://www.sjsu.edu/senate/docs/S12-7.pdf>, requires students to obtain instructor's permission to record the course and the following items to be included in the syllabus:

“Common courtesy and professional behavior dictate that you notify someone when you are recording him/her. You must obtain the instructor's permission to make audio or video recordings in this class. Such permission allows the recordings to be used for your private, study purposes only. The recordings are the intellectual property of the instructor; you have not been given any rights to reproduce or distribute the material.”

- o It is suggested that the greensheet include the instructor's process for granting permission, whether in writing or orally and whether for the whole semester or on a class by class basis.
- o In classes where active participation of students or guests may be on the recording, permission of those students or guests should be obtained as well.

“Course material developed by the instructor is the intellectual property of the instructor and cannot be shared publicly without his/her approval. You may not publicly share or upload instructor generated

material for this course such as exam questions, lecture notes, or homework solutions without instructor consent.”

Academic integrity

Your commitment, as a student, to learning is evidenced by your enrollment at San Jose State University. The [University Academic Integrity Policy S07-2](http://www.sjsu.edu/senate/docs/S07-2.pdf) at <http://www.sjsu.edu/senate/docs/S07-2.pdf> requires you to be honest in all your academic course work. Faculty members are required to report all infractions to the office of Student Conduct and Ethical Development. The [Student Conduct and Ethical Development website](http://www.sjsu.edu/studentconduct/) is available at <http://www.sjsu.edu/studentconduct/>.

San Jose State University Electrical Engineering Department EE Department Honor Code

The Electrical Engineering Department will enforce the following Honor Code that must be read and accepted by all students.

"I have read the Honor Code and agree with its provisions. My continued enrollment in this course constitutes full acceptance of this code. I will NOT:

- 1. Take an exam in place of someone else, or have someone take an exam in my place*
- 2. Give information or receive information from another person during an exam*
- 3. Use more reference material during an exam than is allowed by the instructor*
- 4. Obtain a copy of an exam prior to the time it is given*
- 5. Alter an exam after it has been graded and then return it to the instructor for re-grading*
- 6. Leave the exam room without returning the exam to the instructor."*

Measures Dealing with Occurrences of Cheating

Department policy mandates that the student or students involved in cheating will receive an "F" on that evaluation instrument (paper, exam, project, homework, etc.) and will be reported to the Department and the University.

A student's second offense in any course will result in a Department recommendation of suspension from the University.

Campus Policy in Compliance with the American Disabilities Act

If you need course adaptations or accommodations because of a disability, or if you need to make special arrangements in case the building must be evacuated, please make an appointment with me as soon as possible, or see me during office hours. [Presidential Directive 97-03](http://www.sjsu.edu/president/docs/directives/PD_1997-03.pdf) at http://www.sjsu.edu/president/docs/directives/PD_1997-03.pdf requires that students with disabilities requesting accommodations must register with the [Accessible Education Center](http://www.sjsu.edu/aec) (AEC) at <http://www.sjsu.edu/aec> to establish a record of their disability.

Accommodation to Students' Religious Holidays

San José State University shall provide accommodation on any graded class work or activities for students wishing to observe religious holidays when such observances require students to be absent from class. It is the responsibility of the student to inform the instructor, in writing, about such holidays before the add deadline at the start of each semester. If such holidays occur before the add deadline, the student must notify the instructor, in writing, at least three days before the date that he/she will be absent. It is the responsibility of the instructor to make every reasonable effort to honor the student request without penalty, and of the student to make up the work missed. See [University Policy S14-7](http://www.sjsu.edu/senate/docs/S14-7.pdf) at <http://www.sjsu.edu/senate/docs/S14-7.pdf>.

In general, student requests will be accommodated by allowing early submission of work before the holiday.

SJSU Writing Center

The SJSU Writing Center is located in Clark Hall, Suite 126. All Writing Specialists have gone through a rigorous hiring process, and they are well trained to assist all students at all levels within all disciplines to become better writers. In addition to one-on-one tutoring services, the Writing Center also offers workshops every semester on a variety of writing topics. To make an appointment or to refer to the numerous online resources offered through the Writing Center, visit the [Writing Center website](#) at <http://www.sjsu.edu/writingcenter>. For additional resources and updated information, follow the Writing Center on Twitter and become a fan of the SJSU Writing Center on Facebook. (Note: You need to have a QR Reader to



scan this code.)

SJSU Counseling Services

The SJSU Counseling Services is located on the corner of 7th Street and San Fernando Street, in Room 201, Administration Building. Professional psychologists, social workers, and counselors are available to provide consultations on issues of student mental health, campus climate or psychological and academic issues on an individual, couple, or group basis. To schedule an appointment or learn more information, visit [Counseling Services website](#) at <http://www.sjsu.edu/counseling>.

EE287 / CMOS ASIC Design, S'18, Course Schedule

The following are the intended topics for discussion. The class often gets ahead of the following topics, and then reviews.

The items labeled QUIZ are Canvas quizzes (online quizzes) each students should perform outside of class online. There may be unscheduled quizzes during the semester. The items labeled HW are homework assignments. The homework assignments can be found and must be turned in on the [Canvas System](#).

In class quizzes are not scheduled. Quizzes may be announced on Canvas which are not on this schedule. A password obtained in class may be required.

Dates and assignments can change with class notice. Please check on Canvas for each assignment.

Course Schedule

Week	Date	Topics, Readings	Assignments, Deadlines
1	01/25/2018	intro296.pdf, CMOSASIC2000.pdf, CMOS gate review	cmosgr.pdf
2	01/30/2018	Delay in CMOS overview	cmosdelay.pdf, Verilog Self Test
	02/01/2018	Cell types in 260	260c_pri_e.pdf, HW1 economic analysis
3	02/06/2018	Latches and FFs	latches.pdf QUIZ 1
	02/08/2018	The clock cycle and paths	clkcycle.pdf ,Synthesis HW, Verilog Tutorial
4	02/13/2018	Working with latches	Discussion QUIZ 2, Choose Groups
	02/15/2018	Multiple clock Domains	200Mhz HW,First Design block diagram
5	02/20/2018	Fifos	QUIZ 3
	02/22/2018	Fixing Long Paths and Races	examples, discussion
6	02/27/2018	Working with timing	First Design HW, QUIZ 4
	03/01/2018	A real library	260c_highpri_e.pdf, 300 Mhz HW
7	03/06/2018	Delay models	260c_pri_e.pdf, Paper how to time logic
	03/08/2018	Timing closure	Place and Route HW
8	03/13/2018	Midterm	Study guide
	03/15/2018	Clock distribution networks	Paper -- How to fix timing problems.
9	03/20/2018	Clock generation, PLLs	
	03/22/2018	Product debug requirements	
10	03/27/2018	No Class – Spring Recess	
	03/29/2018	No Class – Spring Recess	
11	04/03/2018	I/O pads and packaging	260e_mac_e.pdf I/O pages, P16,17
	04/05/2018	Power and Ground pins	Engine HW
12	04/10/2018	Power estimation	
	04/12/2018	Floor plan and impacts	QUIZ 5 Power and ground pins
13	04/17/2018	Manf and test. D algorithm	faults.pdf

	04/19/2018	Scan based testing & D algorithm	
14	04/24/2018	Scan based testing	
	04/26/2018	PRN & CRC	
15	05/01/2018	Scan, PRN overview	HW 5 D-Algorithm
	05/03/2018	Bist -- Concepts	HW6
16	05/08/2018	Bist – logic, and Memory	Project submission
	05/10/2018	Final Review	
Final Exam	05/17/2018	19:45-22:00	