San José State University
Electrical Engineering Department
EE279 Topics – Digital System Verification, Spring 2018

Course and Contact Information

Instructor:	Morris Jones
Office Location:	E295 (It's a lab, knock)
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Office Hours:	T & Th 4:30-5:30 (F by appointment)
Class Days/Time:	Tu&Th 6:00PM - 7:15PM
Classroom:	E345
Prerequisites:	Some knowledge of System Verilog

Course Format

Technology Intensive, Hybrid, and Online Courses

The class is taught in a class room. The Canvas online learning system http://sjsu.instructure.com is used extensively for homework information and submission.

Course Description

This course covers topics in verification with the full System Verilog language. Major topics include classes and objects, random constrained test generation, and system-level verification. System Verilog design hierarchy, data types, assertions, interfaces, verification constructs, and test bench structures. Industry tools will be used to illustrate principles taught. Overall concepts will be tied together by verification projects using UVM. Project team work will be stressed.

Course Learning Outcomes (CLO) (Required)

Upon successful completion of this course, students will be able to:

- LO1 Utilize classes to encapsulate verification mechanisms
- LO2 Utilize objects to allow code reuse and extension
- LO3 Create service classes to perform common verification functions
- LO4 Use different memory types for efficient verification and modeling
- LO5 Generate verification cases using constrained random variables
- LO6 Comprehend and obtain DUT code coverage metrics
- LO7 Understand and explain the UVM block diagram and organization
- LO8 Demonstrate the ability to create comprehensive SV module verification platforms

Required Texts/Readings

Textbook

There is no textbook for EE279. The course is taught from industry documents and specifications. These are available on the Canvas system.

Other Readings

Supplementary materials are also found on the Canvas system

Other technology requirements / equipment / material

Students will require access to state of the art engineering tools. These are provided at SJSU in the E289 and E291 labs. Students may access the labs remotely. Other tools may be used in project development, but all homework must be run with the required scripts in the SJSU labs before submission.

Course Requirements and Assignments

The course will have homework assignments, quizzes, projects and exams. These are listed in detail in the Canvas system.

Final Examination or Evaluation

The course has a final exam. It is during the normal final exam times. The exam is comprehensive. It includes theory, recall, and coding questions.

Grading Information

Grading is outcome based. Grades will not be adjusted to solve student Grade issues. You get what you earn! No exceptions are granted. It is important to keep up and apply yourself consistently during the semester.

Homework (15%): Homework will consist of a mix of analysis , design, and documentation problems. Analytical and CAD based techniques will be required to solve problems. The homework is designed to reinforce lecture concepts and prepare the student for the exams and class project. Homework assignments will be due according to the green sheet. Online and in class assessments (quizzes) are included in the homework scores. In class quizzes are not scheduled or announced.

All homework shall be submitted individually using online systems. You can scan documents at the academic success center

Individual homework will be checked for possibly copying. Homework that demonstrates plagiarism will receive a score of '0'. Note that translation or modest changes are considered plagiarism. No consideration will be made for who copied who.

Developing professional discipline through on time homework submission is expected and required. The Canvas system will not inform you an assignment is late. Homework is not accepted late. Homework must be submitted through the electronic system. No homework is accepted on paper, through email, or other means. The canvas system has no provision allowing late submission for a single student.

Several homework assignments require design and debug. Students are required to analyze the assignments, and start early enough to complete the assignments according to the schedule.

10% Class project. The project is a design/verification problem. The specifications will be found on Canvas. Teams of 2-3 people are expected to work on the problem. The project will not be accepted late. A maximum of 50% of the homework score can be earned if the design does not pass/verify tests. To discourage *borrowing* of other designs, successful designs will be run through a recursive difference engine, and the score will be reduced to zero if similar in any significant way to other submitted designs. Both design teams will be penalized. The instructor will not attempt to determine which design was copied. Don't share project designs.

Midterm (30%): Covers the first half of the semester. All exams are closed book, no notes. Scratch paper will be provided during the exam. You will be seated randomly in the class, and there may be multiple versions of the exam. You should bring a calculator and writing instruments to the exam. Programmable calculators are not allowed unless completely cleared. Cell phones may not be used in exams. Photo ID is required when you turn in your exam. Exams are a mix of theory, design, coding, and computation.

Final Exam (45%): The final exam will be the same format as the midterm except it will cover the entire semester with emphasis on the last half of the semester. The rules are the same as the midterm

Determination of Grades

Grade	%	Comment
A	100%	May vary down from 100%
A-	90 – 99.999%	May vary down from 99.999%
B/+/-	80-89.9999%	varies for + and -
C+	78-79.99999%	No C or C- grades are typically given
F	0-77.99999%	

The +/- grade breaks are set by adjusting the thresholds up and down to meet the department grade distribution guidelines. The break points will not be known until the semester is over, and the class composite scores are available.

Classroom Protocol

Students will turn their cell phones off or put them on vibrate mode while in class. They will not answer their phones in class. Students whose phones disrupt the course and do not stop when requested by the instructor will be referred to the Judicial Affairs Officer of the University. Students are expected to attend all classes. There is no follow along text book. If you will miss a class, get the materials from another student. The professor will not reteach missed lectures during office hours due to time limitations.

Common courtesy and professional behavior dictate that you notify someone when you are recording him/her. You must obtain the instructor's permission to make audio or video recordings in this class. Such permission allows the recordings to be used for your private, study purposes only. The recordings are the intellectual property of the instructor; you have not been given any rights to reproduce or distribute the material.

- In classes where active participation of students or guests may be on the recording, permission of those students or guests should be obtained as well.

Course material developed by the instructor is the intellectual property of the instructor and cannot be shared publicly without his/her approval. You may not publicly share or upload instructor generated material for this course such as exam questions, lecture notes, or homework solutions without instructor consent.

University Policies

Per University Policy S16-9, university-wide policy information relevant to all courses, such as academic integrity, accommodations, etc. will be available on Office of Graduate and Undergraduate Programs' Syllabus Information web page at http://www.sjsu.edu/gup/syllabusinfo/"

The Electrical Engineering Department will enforce the following Honor Code that must be read and accepted by all students.

"I have read the Honor Code and agree with its provisions. My continued enrollment in this course constitutes full acceptance of this code. I will NOT:

1. *Take an exam in place of someone else, or have someone take an exam in my place*
2. *Give information or receive information from another person during an exam*
3. *Use more reference material during an exam than is allowed by the instructor*
4. *Obtain a copy of an exam prior to the time it is given*
5. *Alter an exam after it has been graded and then return it to the instructor for re-grading*
6. *Leave the exam room without returning the exam to the instructor."*

Measures Dealing with Occurrences of Cheating

1. *Department policy mandates that the student or students involved in cheating will receive an "F" on that evaluation instrument (paper, exam, project, homework, etc.) and will be reported to the Department and the University.*
2. *A student's second offense in any course will result in a Department recommendation of suspension from the University.*

EE279 / Topics – Digital System Verification, Spring 17, Course Schedule

Course Schedule

Week	Date	Topics, Readings, Assignments, Deadlines
1	01/25/2018	Introduction,,Intro.pdf
2	01/30/2018	Verilog Review/ SV classes,,LRM 20
2	02/01/2018	Data types, Memory types,Quiz Ch 20,LRM 4, 5
3	02/06/2018	Class methods, functions, objects Rand Intro,Quiz Ch 4, Quiz Ch 5,LRM 7
3	02/08/2018	Verification Concepts,Random numbers HW,Quiz Ch 7
4	02/13/2018	UVM Overview,,Notes
4	02/15/2018	Components, driver classes,ALU sequence HW,LRM 10
5	02/20/2018	Random Constraints,,LRM 13, quiz Ch 13
5	02/22/2018	Constraint in class examples,ALU driver HW,LRM 13
6	02/27/2018	Messages and processing,,LRM 14
6	03/01/2018	Inter process Communications,Monitor HW,LRM 14
7	03/06/2018	Developing UVM tests
7	03/08/2018	Pictures and tools in UVM development,
8	03/13/2018	Multiple monitors and reuse,LRM 16
8	03/15/2018	Midterm review,,
9	03/20/2018	Midterm,,
9	03/22/2018	Developing test environments

10	03/27/2018	***No Class – Spring Recess***
10	03/29/2018	***No Class – Spring Recess***
11	04/03/2018	Project Introduction,,Notes
11	04/05/2018	Project discussion,,Test case HW
12	04/10/2018	Scoreboard divisions,,
12	04/12/2018	Post simulation analysis,,
13	04/17/2018	Coverage Blocks,,LRM 18, Project test strategy and template
13	04/19/2018	Coverage Blocks,Multiplier coverage,LRM 18
14	04/24/2018	Services,,LRM 21
14	04/26/2018	*UVM Component review, test cases 1 and 2 submission*
15	05/01/2018	UVM Parameters, passing data around
15	05/03/2018	UVM routines,test cases 3 and 4 submission
16	05/08/2018	Getting test parameters,,
16	05/10/2018	Final Review
Final Exam	05/17/2018	17:15-19:30