San José State University
College of Engineering

EE278 Digital Design for DSP and ~~Communications~~ AI/DNN
Fall 2017, Section 3

Instructor:	Prof. Chang "Charles" Choo
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Office Hours:	Tue,1:30pm-2:30pm, Fri, 2pm-3pm
Class Days/Time:	Fri, 3pm-5:45pm
Classroom:	ENG 345
Prerequisites:	EE EE270 (or EE271), EE253 (or EE153) or equivalent. Knowledge of programming language (C/C++, Matlab and/or Simulink), hardware description language (Verilog or VHDL), and basic DSP theory.

Course Format:
This course provides an in-depth and state-of-the-art coverage on the design and VLSI/FPGA/ASIC-based implementation of high-performance DSP/DNN systems. After presenting FPGA architectures and design tools by Altera (and/or Xilinx), several design examples on DSP, video/imaging, and AI will be covered, including 1-D/2-D FIR filters, image processing algorithm blocks, and CNN (Convolutional Neural Network).
There will be 4-5 mini-projects.

Required Texts
Altera DE1 Board, http://www.terasic.com.tw/cgi-bin/page/archive.pl?Language=English&CategoryNo=53&No=83 , provided by DSP/FPGA Lab.

Intel/Altera DE0-Nano-SoC Kit/Atlas-SoC Board.(http://www.terasic.com.tw/cgi-bin/page/archive.pl?Language=English&CategoryNo=167&No=941), $90 with academic discount.

Handouts in soft copy will be occasionally posted on Canvas.

References

1. Uwe Meyer-Baese, Digital Signal Processing with Field Programmable Gate Array, 2nd Ed., Springer-Verlag, New York, 2004 (ISBN 3-540-21119-5). 1st Ed. is fine too. On-line purchase through, e.g., amazon.com, suggested.
2. C.Y. Choo, FPGA DSP System Design, (Lecture slides & writing), August 2014 (Available in Maple Press).
3. Altera DE0-Nano-SoC Kit/Atlas-SoC Board Website.
4. ZYBO Zynq™-7000 Development Board and Xilinx University Program Website (Available at Digilent, http://digilentinc.com/Products/Detail.cfm?NavPath=2,400,1198&Prod=ZYBO)
5. C.Y. Choo (ed.), Reference Manual for FPGA System Design Using Altera DE Board, August 2011 (Draft 2.0). Out of print.
6. The Verilog Golden Reference Guide, by Doulos, 1996.
7. Won Yang, Yong Cho, Chang Choo, et al., MATLAB/Simulink for Digital Signal Processing, on-line purchase through amazon.com available.

Web site

Class information, notices, course materials, FAQs (selected course related emails between students and Instructor) will be posted on Canvas. In addition, all the changes on the tentative list of homework problems (see below), as well as solutions to homework, will be available on the Canvas. Students are urged to visit the web site twice a week.

Exams and Assignments

There will be one midterm and one final exam. The midterm dates will be announced at least 1 week before the exam. The final exam will be given at the official university final exam time for this course. There will be 4-5 mini-projects and 5-7 assignments.

Office Hours

The office hours are made available for questions about lectures and projects and for discussion of grades assigned. If you need a help of the instructor, see him right after class or during his office hours (Tue, 1:30pm-2:30pm, Fri, 2pm-3pm). Use of email is strongly recommended for other times, although appointments may be made for mutually convenient times.

Grading Policy

The weighting among exams, assignments, and homework will be:

Mini-projects (4-5)	45%
Homework	10%
Midterm Exam	15%
Final Exam	30%

Tentative Schedule

Mini-projects:

1	Pipelined Floating-Point Adder Design (Due: TBD)
2	FIR Filter Design on Logic Fabric (Due:TBD)
3	Matrix Multiplier Design on Logic Fabric (Due:TBD)
4	Simple CNN Design on Logic Fabric (Due:TBD)
5	CNN on HPC (Due:TBD)

Class:

Lecture	Date	Topic
1	8/25	Introduction, Arithmetic Circuit Review
2	9/1	DSP Arithmetic
3	9/8	FPGA DSP System Design Flow
4	9/15	FPGA Architecture
5	9/22	FIR Filter Design, 2D Convolution
5	9/29	Artificial Intelligence/Machine Learning: Theory
6	10/6	CNN Architectures
	10/13	Midterm
7	10/20	Embedded Processing System Design
8	10/27	OpenCL on FPGAs
9	11/3	Heterogeneous Computing (GPGPU/FPGA)
10	11/10	Adaptive FIR Filter
11	11/17	High Performance Computing with FPGA & GPGPU, Data Center
	11/24	Thanksgiving
12	12/1	Student Presentation (Miniprojects 4&5) and Evaluation
13	12/8	Review
		Final Exam