San José State University
Charles W. Davidson College of Engineering/Department of Electrical Engineering
EE 277A, Embedded SoC Design, Spring 2018

Course and Contact Information

Instructor:	Youngsoo Kim
Office Location:	Engineering Building Room 363
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Email:	youngsoo.kim@sjsu.edu
Office Hours:	Monday and Wednesday 3-4PM
Class Days/Time:	Tuesday, and Thursday 4:30-5:45PM
Classroom:	ENG 395 and Lab 389
Prerequisites:	EE 210 *Linear System Theory (can be taken concurrently)* or instructor's consent

MYSJSU Messaging

Course materials such as syllabus, handouts, notes, assignment instructions, etc. can be found on Canvas Leaning Management System course login website at http://sjsu.instructure.com. Students are responsible for regularly checking with the messaging system through MySJSU at http://my.sjsu.edu to learn of any updates.

Course Description

Embedded system design challenge and metrics. Processor and compiler technologies. Software and hardware architectures for embedded system design. The design of co-processors, parallel processors, graphic processors and MPSOC processors. Basic concepts of high performance computing (HPC).

Course Learning Outcomes (CLO)

Upon successful completion of this course, students will be able to:

1. Describe in reasonable details architecture of a high performance embedded system.
2. Perform a detailed design of a high performance embedded system design based on SIMD co-processors, and Field Programmable Gate Array (FPGA) accelerators.
3. Design and develop parallel software on graphic processors
4. Design and develop system software including compiler backend and real-time OS.
5. Design server based High Performance Computing (HPC) systems to accelerate application algorithms at the orders of magnitude.

Required Texts/Readings

Textbook

1. High Performance Embedded Computing : Architectures, Applications, and Methodologies, Second Edition, Marilyn Wolf, Morgan Kaufmann, 2014 (eBooks available through SJSU Library)
2. ZYBO Zynq™-7000 Development Board and Xilinx University Program Website (Available at Digilent at http://digilentinc.com/Products/Detail.cfm?NavPath=2,400,1198&Prod=ZYBO)
3. Lecture and lab handouts

Other Readings

1. Embedded Systems Embedded Systems, 1st Edition, ARM Programming and Optimization, J. Bakos, Morgan Kaufmann, ISBN 9780128004128 (eBooks available through SJSU Library)
2. Koenig, Andrew. C Traps and Pitfalls. Reading, Mass.: Addison-Wesley, 1988.

Course Requirements and Assignments

There will be one midterms and one final exam. The midterm dates will be announced at least 1 week before the exam. Four laboratory projects and a final presentation will be assigned. The report grades will be based on a written report and a lab demonstration.

Student who turn in identical report, and/or source code will be considered to have copied. Two hundred percent (-200%) of the maximum possible grade will be deducted for each instance of cheating on laboratory assignments. Copying of material from the Web or other students for laboratory reports and/or source code is considered to be an act of cheating. Illegal copying or cheating on an exam or on the laboratory assignments will result in a -200% for that exam or for the project. All the provisions of the code of student conduct apply to this course as appropriate.

Final Examination

The final exam will be given at the official university final exam time for this course.

Grading Information

Assignment	Weight
Lab projects, and final presentation	40%
In-class quizzes, and/or homework assignments	5%
Midterm exam	25%
Final exam	30%

Determination of Grades

Letter grades will be assigned based on the distribution curves for final raw score.

Percentage Grade	Letter Grade
97% and above	A+
94% - 96%	A

90% - 93%	A-
87% - 89%	B+
83% - 86%	B
80% - 82%	B-
77% - 79%	C+
73% - 76%	C
70% - 72%	C-
67% - 69%	D+
63% - 66%	D
60% - 62%	D-
Below 59%	F

University Policies

Per University Policy S16-9, university-wide policy information relevant to all courses, such as academic integrity, accommodations, etc. will be available on Office of Graduate and Undergraduate Programs' Syllabus Information web page at http://www.sjsu.edu/gup/syllabusinfo/

EE Honor Code - Honesty and Respect for Others and Public Property

The Electrical Engineering Department will enforce the following Honor Code that must be read and accepted by all students.

"I have read the Honor Code and agree with its provisions. My continued enrollment in this course constitutes full acceptance of this code. I will NOT:

- Take an exam in place of someone else, or have someone take an exam in my place
- Give information or receive information from another person during an exam
- Copy project information from others
- Use more reference material during an exam than is allowed by the instructor
- Obtain a copy of an exam prior to the time it is given
- Alter an exam after it has been graded and then return it to the instructor for re-grading
- Leave the exam room without returning the exam to the instructor."

Measures Dealing with Occurrences of Cheating

Department policy mandates that the student or students involved in cheating will receive an "F" on that evaluation instrument (paper, exam, project, homework, etc.) and will be reported to the Department and the University. A student's second offense in any course will result in a Department recommendation of suspension from the University.

EE 277A / Embedded SoC Design, Spring 2018, Course Schedule

Schedule is subject to change with fair notice by email and class announcement.

Course Schedule

Week	Date (2018)	Topics, Readings, Assignments, Deadlines
1	1/25	Course Introduction
2	1/30-2/1	Chap. 1. Embedded Computing, Design methodologies
3	2/6-8	Parallel language introduction , OpenMP, and lab
4	2/13-15	OpenACC introduction, and lab
5	2/20-22	MPI introduction, and lab
6	2/27-3/1	Hybrid computing, Lab assignment
7	3/6-8	Chap 2. VLIW, SIMD Processors
8	3/13-15	Midterm review **, Midterm Exam (subject to change)**
9	3/20-22	Chap 2 (cont'd), Configurable Processor
10	3/27-29	Spring Recess (no class)
11	4/3-5	Chap 3. Program , SD SoC, and lab introduction
12	4/10, 12, 13	Chap 4. OS, Zybo OS lab introduction
13	4/17	Zybo OS lab
14	4/24-26	Chap 5. MpSoC, NoC
15	5/1-3	Chap 7. HW/SW Co-design intro
16	5/8-10	Final Presentation
Final Exam	5/17	14:45-17:00PM