San José State University
Electrical Engineering
EE272, SOC design, Spring, 2018

Course and Contact Information

Instructor:	Morris Jones
Office Location:	E295 (It's a lab, knock)
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Office Hours:	M & W 4:30-5:30PM (F by appointment)
Class Days/Time:	M & W 7:30-8:45PM
Classroom:	E341
Prerequisites:	EE 271-Advanced Digital System Design and Synthesis (or instructor's consent); self-motivation in learning EDA tools, Hardware Design and Verification Languages

Course Format

Technology Intensive, Hybrid, and Online Courses

The class is taught in a class room. The Canvas online learning system http://sjsu.instructure.com is used extensively for quizzes, homework information and submission.

Course Description

This course covers topics in System-on-Chip design and verification with SystemVerilog. Major topics include top-down SoC design and SoC buses; design for reuse and integration; IP integration and system-level verification and synthesis; SystemVerilog design hierarchy, data types, assertions, interfaces, verification constructs, and testbench structures. Design integration and verification will be stressed. Industry tools will be used to illustrate principles taught. Overall concepts will be tied together by design projects. Project team work will be stressed.

Course Learning Outcomes (CLO) (Required)

Upon successful completion of this course, students will be able to:

- LO1. Understand SoC design methodology to various application specifications
- LO2. Apply SoC design flow for a specific SoC design project
- LO3. Partition and map an application specification to SoC architecture
- LO4. Develop and use of SoC buses for a SoC design
- LO5. Perform system-level synthesis, which includes binding, scheduling, and resource sharing
- LO6. Design and implement different types of IP cores based on required specifications

- LO7. Design a SoC by IP integration method
- LO8. Model and verify a design by SystemVerilog language
- LO9. Develop testbenches with SystemVerilog HVL for SoC verification

While not a stated learning objective, students will practice Verilog/SystemVerilog skills through assignments and projects.

A course goal is students learn to enjoy the SOC design team experience through a *hands on* approach.

Required Texts/Readings

Textbook

All materials are available on the Canvas learning system.

Other technology requirements / equipment / material

The labs in E289 and E291 will be used for most homework assignments.

Course Requirements and Assignments

The course has many quizzes. These are primarily in the online Canvas system. Lab homework is turned in on Canvas. There are two team projects. There will be a midterm, and a final.

Final Examination or Evaluation

The final examination is comprehensive, and held during the final exam time. The exam consists of theory questions, recall questions, and coding questions.

Grading Information

Grading is outcome based. Grades will not be adjusted to solve student Grade issues. You get what you earn! No exceptions are granted. It is important to keep up and apply yourself consistently during the semester.

- Homework (15%): Homework will consist of a mix of analysis , design, and documentation problems. Analytical and CAD based techniques will be required to solve problems. The homework is designed to reinforce lecture concepts and prepare the student for the exams and class project. Homework assignments will be due according to the green sheet. Online and in class assessments (quizzes) are included in the homework scores. In class quizzes are not scheduled or announced.
    - All homework shall be submitted individually using online systems. Instructions are at http://sjsu.instructure.com You can scan documents at the academic success center
        - Individual homework will be checked for possibly copying. Homework that demonstrates plagiarism will receive a score of '0'. Note that translation or modest changes are considered plagiarism. No consideration will be made for who copied who.
    - Developing professional discipline through on time homework submission is expected and required. The canvas system will not inform you an assignment is late. Homework is not accepted late. Homework must be submitted through the electronic system. No homework is accepted on paper, through email, or other means. Submitting late homework in a later assignment slot will receive no score. The canvas system has no provision allowing late submission for a single student. If you will be out of town, submit homework early,
    - Several homework assignments require design and debug. Students are required to analyze the assignments, and start early enough to complete the assignments according to the schedule.
- 15% Class project. The project is a design/verification problem. The specifications will be found on Canvas. Teams of 2-3 people are expected to work on the problem. The project will not be accepted late. A maximum of 50% of the homework score can be earned if the design does not pass the tests. To discourage *borrowing* of other designs, successful designs will be run through a recursive difference engine, and the score will be reduced to zero if similar in any significant way to other submitted designs. Both design teams will be penalized. The instructor will not attempt to determine which design was copied. Don't share project designs.

- Midterm (25%): Covers the first half of the semester. All exams are closed book, no notes. Scratch paper will be provided during the exam. You will be seated randomly in the class, and there may be multiple versions of the exam. You should bring a calculator and writing instruments to the exam. Programmable calculators are not allowed unless completely cleared. Cell phones may not be used in exams. Photo ID is required when you turn in your exam. Exams are a mix of theory, design, coding, and computation.
- Final Exam (45%): The final exam will be the same format as the midterm except it will cover the entire semester with emphasis on the last half of the semester. The rules are the same as the midterm

Determination of Grades

Grade	%	Comment
A	100%	May vary down from 100%
A-	90 – 99.999%	May vary down from 99.999%
B/+/-	80-89.9999%	varies for + and -
C+	78-79.99999%	No C or C- grades are typically given
F	0-77.99999%	

The +/- grade breaks are set by adjusting the thresholds up and down to meet the department grade distribution guidelines. The break points will not be known until the semester is over, and the class composite scores are available. They will not be higher than this breakdown.

Classroom Protocol

Students will turn their cell phones off or put them on vibrate mode while in class. They will not answer their phones in class. Students whose phones disrupt the course and do not stop when requested by the instructor will be referred to the Judicial Affairs Officer of the University. Students are expected to attend all classes. There is no follow along text book. If you will miss a class, get the materials from another student. The professor will not reteach missed lectures during office hours due to time limitations.

Common courtesy and professional behavior dictate that you notify someone when you are recording him/her. You must obtain the instructor's permission to make audio or video recordings in this class. Such permission allows the recordings to be used for your private, study purposes only. The recordings are the intellectual property of the instructor; you have not been given any rights to reproduce or distribute the material.

- In classes where active participation of students or guests may be on the recording, permission of those students or guests should be obtained as well.

Course material developed by the instructor is the intellectual property of the instructor and cannot be shared publicly without his/her approval. You may not publicly share or upload instructor generated material for this course such as exam questions, lecture notes, or homework solutions without instructor consent.

University Policies

Per University Policy S16-9, university-wide policy information relevant to all courses, such as academic integrity, accommodations, etc. will be available on Office of Graduate and Undergraduate Programs' Syllabus Information web page at http://www.sjsu.edu/gup/syllabusinfo/"

The Electrical Engineering Department will enforce the following Honor Code that must be read and accepted by all students.

"I have read the Honor Code and agree with its provisions. My continued enrollment in this course constitutes full acceptance of this code. I will NOT:

1. *Take an exam in place of someone else, or have someone take an exam in my place*
2. *Give information or receive information from another person during an exam*
3. *Use more reference material during an exam than is allowed by the instructor*
4. *Obtain a copy of an exam prior to the time it is given*
5. *Alter an exam after it has been graded and then return it to the instructor for re-grading*
6. *Leave the exam room without returning the exam to the instructor."*

Measures Dealing with Occurrences of Cheating

1. *Department policy mandates that the student or students involved in cheating will receive an "F" on that evaluation instrument (paper, exam, project, homework, etc.) and will be reported to the Department and the University.*
2. *A student's second offense in any course will result in a Department recommendation of suspension from the University.*

EE272 / Soc Design, Fall 2018, Course Schedule

The following are the intended topics for discussion. The class often gets ahead of the following topics, and then reviews..The items labeled QUIZ are canvas quizzes (online quizzes) each students should perform outside of class online. The quizzes may include prior materials. There may be unscheduled quizzes during the semester. The items labeled Design and HW are homework assignments. The homework assignments can be found and are turned in on the canvas system http://sjsu.instructure.com

Dates and assignments may change with class notice.

Course Schedule

Week	Date	Topics, Readings, Assignments, Deadlines
1	01/24/2018	Verilog Review/ SV interfaces,,Intro.pdf, LRM 3,4
2	01/29/2018	Soc Concepts, reuse & integration,Quiz Ch 3,LRM 5,20,
2	01/31/2018	Structures/ always * blocks,Quiz Ch 5,SoCOverview.pdf,
3	02/05/2018	Busses – Master-slave,Quiz Ch 20,LRM 4-10, 4-11
3	02/07/2018	Structures,,Bus notes
4	02/12/2018	AHB,Quiz Ch 4,LRM 4-10, 4-11, 4-13,
4	02/14/2018	Assignment operators,Design HW 1,
5	02/19/2018	Message Passing/Rings,,LRM 8,
5	02/21/2018	Unions, Designing for reuse, IP standards,,Bus notes
6	02/26/2018	Packet based busses,Quiz Ch 8,LRM 4-11, notes
6	02/28/2018	Port Connections,,Packet notes, Design HW 2
7	03/05/2018	Error Handling,,LRM 19,20
7	03/07/2018	Assertions,Quiz Ch 19,Error notes
8	03/12/2018	Midterm,,Midterm study guide

Week	Date	Topics, Readings, Assignments, Deadlines
8	03/14/2018	Looping Controls,Design HW 3,
9	03/19/2018	Mult-master/Split transactions,,Quiz Ch 10, LRM 9
9	03/21/2018	Final Project discussion,Assertions,
10	03/26/2018	***No class --- Spring Recess***
10	03/28/2018	***No class --- Spring Recess***
11	04/02/2018	Fairness Techniques/ QOS 1,Quiz Ch 9,LRM 8
11	04/04/2018	Covergroups,,Scheduling notes
12	04/09/2018	File I/O,Quiz Ch 17,Scheduling notes
12	04/11/2018	Verification,,LRM 22
13	04/16/2018	Misc SV,Binary Tree,Verification notes
13	04/18/2018	Test Bench concepts,Covergroups,LRM *, LRM 7
14	04/23/2018	Classes,,Test bench notes
14	04/25/2018	Voting/budget based,, LRM 7
15	04/30/2018	Fifos / bandwidth smoothing,,Fairness notes
15	05/02/2018	Fifos / bandwidth smoothing,Bus design,Fifo notes
16	05/07/2018	Verification part 2
16	05/09/2018	Project Results Presentation, Design HW Project
	05/14/2018	Final Review, Study guide
Final	05/16/2018	19:45-22:00