San José State University
Charles W. Davidson College of Engineering
DEPARTMENT OF ELECTRICAL ENGINEERING

EE271-01 - Advanced Digital System Design and Synthesis (Fall 2017)

Course and Contact Information

Instructor:	John (JeongHee) Kim PhD
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Office Hours:	Monday & Wednesday, 16:30 – 17:30
Class Days/Time:	Monday & Wednesday, 18:00 – 19:15
Classroom:	Engineering Building, room 339
Prerequisites:	Graduate standing. Experiences in digital/logic design. Background in integrated circuit design is helpful. Must have self-motivations in **self-learning EDA tools** and Verilog HDL

Faculty Web Page and MYSJSU Messaging

Course materials such as syllabus, handouts, notes, assignment instructions, etc. can be found on the website at https://groups.yahoo.com/groups/SJSU_EE271. You are responsible for regularly checking with your official email address (email address stored on your MySJSU account) and the messaging system through your MySJSU at http://my.sjsu.edu to learn of any updates from the course instructor.

Course Description

This course covers topics in the advanced design and analysis of digital circuits with HDL. The primary goal is to provide in depth understanding of logic and system design, synthesis, and optimization for area, speed and power consumption. The course enables students to apply their knowledge for the design of advanced digital hardware systems with corresponding EDA tools. Verilog HDL will be used for simulation and synthesis of the homework assignments and final design project.

Course Learning Outcomes

Upon successful completion of this course, students will be able to:

CLO 1. Design and manually optimize complex combinational and sequential digital circuits
CLO 2. Model combinational and sequential digital circuits by Verilog HDL
CLO 3. Design and model digital circuits with Verilog HDL at the algorithm (behavioral) and data flow (RTL) levels as well as with behavioral and structural languages.

CLO 4. Develop test benches to verify the design by simulation and analysis
CLO 5. Perform functional and timing verifications of digital circuits
CLO 6. Perform static and dynamic timing analysis with false paths and hazards
CLO 7. Synthesis combinational and sequential circuits with trade-offs in timing, area, and power
CLO 8. Understand the relationships between timing performance, parallelizing and pipelining
CLO 9. Understand fundamental principles of analyzing power distribution and optimizing power consumption in digital circuits

Required Texts, Reading Materials, UNIX Accounts and EDA Tools

Textbooks

- Digital Systems Design Using Verilog by Charles Roth, Lizy K. John, Byeong Kil Lee ISBN-13: 978-1285051079 ISBN-10: 1285051076

Additional Readings (optional)

- Any "Verilog Language" books/notes. Below are few on-line documents:
  http://www.doulos.com/knowhow/verilog_designers_guide/
  https://www.nandland.com/
- D. R. Smith and P.D. Franzon, "Verilog Styles for Synthesis," (Pearson Education [Prentice Hall]), 2000.ISBN. 0-201-61860-5
- Michael Keating, David Flynn, Robert Aitken, Alan Gibbons, Kaijian Shi, "Low Power Methodology Manual," Springer 2007. ISBN: 978-0-387-71818-7

UNIX Accounts on Cadence Laboratory

- Rooms E289 and E291 are Cadence laboratories installed with Cadence and Synopsys software tools. Each registered SJSU student should automatically have a UNIX account. If you do not know your login name and password (or having problems with the account), you can find out at https://unix.engr.sjsu.edu/wiki/doku.php
- For Unix tutorial materials and other documents related to Cadence laboratory, please consult Prof. Parent's website at www.sjsu.edu/people/david.parent/

EDA Tools

- Synopsys Verilog Compiler Simulator (VCS) (required): Available on SJSU Cadence Lab
- Synopsys Design Compiler (required): Available on SJSU Cadence Lab
- Cadence NC-Verilog Simulator (optional): Available on SJSU Cadence Lab
- Any other Verilog simulators (such as ModelSim PE (optional), which can be downloaded at http://www.mentor.com/company/higher_ed/modelsim-student-edition

Course Requirements and Assignments

Lectures

The course will follow the selected subjects as listed on the course description. Additional theory and examples will be given and discussed in class as much as time permits.

- Please note that lecture materials are NOT solely based on the required text and so students are responsible for following up the lecture in order to prepare themselves for the exams
- Students are responsible for the reading the text, handouts, lecture presentations, etc.
- Students are responsible for following up and keeping track of the in-class lecture materials.
- Students are responsible for finding and reading additional books, papers, examples, etc. in order to gain more understanding of the materials discussed in the lectures.
- Students are responsible for self-learning and using of EDA tools for assigned homework problems, lab exercises, projects, and for lecture discussions.

Midterm and Final Exams and Design Project

There will be **two midterm exam**, **a comprehensive final exam**, **quizzes, and an individual final design project with report**. The exams (Final exam date is posted by the university) and project due dates will be discussed in the class. Since make-up exams will NOT be allowed, please make sure that you are able to attend all exams at the indicated scheduled dates and times (from the beginning of the semester) in order to register for the course.

 All exams are closed-book exams.

- One sheet (double-side) of hand-written notes is allowed for each midterm exam and two sheets of hand-written notes are allowed for the final exam.
- Summary (printed) of Verilog keywords is allowed. Please download this summary and have it with you during the exam.
- Only basic calculators are allowed.

 There will be no make-up exams

Homework Assignments and Lab Exercises

- Homework assignments and/or lab exercises will be given with due dates
    - **If you turn in assignments late, maximum of 10% credits** will be given. Solutions to the homework assignments and all other info are posted in group site (**https://groups.yahoo.com/groups/SJSU_EE271**). Everyone must join in this site to get necessary info (Exam sol, Qz sol, HW assignments & sol, and other announcements).
- **If 75% of combined HW, quizzes, & attendance are not done by end of semester, you will get F grade automatically**.
    - HW has to have cover page given in the group site otherwise you will not get any credits or deducted up to 100 percent. Final solutions on HW and exam must be boxed. Otherwise you will not get credits. Only one side of page must be used in the HWs. (No HW sending through an email will be accepted.) HW should be clean, legible, stapled on top left corner and proper paper should be used.
- If unreasonable or out of common sense behavior happens in the class, one will be asked to leave from the class and will be given "F" grade. (No feet on a table or chair, taking hat off, no cellphone use or web surfing, no talking with neighbors). And I will drop you from the class if the class is disturbed unreasonably with my right.
- Attendance **will be checked randomly (will be considered as one HW)** and will be counted as part of HW & Qz grading.
- **No food** is allowed (Water is ok). All the exams and quizzes are done in the class and only allowed to use pencil and eraser (no pen)
- Homework must be submitted in class.
- Do NOT submit HW via email. Submit HWs in class as hard-copies (paper) only
- Late submission will NOT be accepted (absolutely!).
- There is no make-up homework/lab To get credit for your homework/lab assignments, submissions must be neat, clean, and must be done professionally and seriously. Your official name (not nickname), course #, and homework # must be visibly shown on each assignment.

Grading Information

The overall course grades (letter-grades) will be assigned based on a defined grading standard as shown below. The weights of the whole course work assignments are:

1. Homework assignments & Labs & Quizzes & Attendance	20% (Quiz=HW=Attendance)
2. Two midterm exams	40% (20% each)
3. One final exam	30%
4. Projects	10%

And the overall course grade (letter-grade) will be assigned based on the distribution below:

Grading criteria (Example: 74% results in a grade of C+):

0<F<57<D-<60<D<64<D+<67<C-<70<C<74<C+<77<B-<80<B<84<B+<87<A-<90<A<100

Classroom Protocol

EE271 students understand that professional attitude is necessary to maintain a comfortable academic environment in the classroom. For examples:

- Students will put their cell phones in quiet/vibration mode during the lecture.
- Students understand that drinking water, juices, etc. during the lecture is acceptable but NOT eating.
- Students will not skip the lecture and then ask the instructor to summarize the lecture later on. Office hours are for students to have questions, not for the instructor to summarize the lecture for any specific student.
- Students will come to the class on time and leave the class at the end of the lecture.
- Students will consult the course syllabus for class policies and requirements before requesting the instructor for any special considerations and/or exceptions
- To minimize possible tension during the exams, students are requested to follow the exam rules closely.
- Students will work on the project and report by their own and will not share the work with other students
- Students understand that long-term learning is their responsibility and will always keep it up.

If you need explanations on lecture materials, projects, homework assignments, exams, etc…, please see me in-person during my office hours. Do NOT email me for these matters. *If you must send me an email, please clearly specify your full-name, course, section, etc. I will not respond to email that I do not know the author or emails that have no manners.*

University Policies

Office of Graduate and Undergraduate Programs **maintains university-wide policy information relevant to all courses, such as academic integrity, accommodations, etc.**" You may find all syllabus related University Policies and resources information listed on GUP's Syllabus Information web page at http://www.sjsu.edu/gup/syllabusinfo/

EE Honor Code - Honesty and Respect for Others and Public Property

The Electrical Engineering Department will enforce the following Honor Code that must be read and accepted by all students.

"I have read the Honor Code and agree with its provisions. My continued enrollment in this course constitutes full acceptance of this code. I will NOT:

- Take an exam in place of someone else, or have someone take an exam in my place

- Give information or receive information from another person during an exam
- Copy project information from others
- Use more reference material during an exam than is allowed by the instructor
- Obtain a copy of an exam prior to the time it is given
- Alter an exam after it has been graded and then return it to the instructor for re-grading Leave the exam room without returning the exam to the instructor."

Measures Dealing with Occurrences of Cheating

- Department policy mandates that the student or students involved in cheating will receive an "F" on that evaluation instrument (paper, exam, project, homework, etc.) and will be reported to the Department and the University.
- A student's second offense in any course will result in a Department recommendation of suspension from the University.

Course Schedule (tentative)

Schedule is subject to change with fair notice by email and class announcement

Tentative Class Schedule (will be updated as needed)			
Week	**Topic**		
Wk 1, 2, 3, 4, 5	**Class information & Introduction**		
		Syllabus, class information and policies	
		• Review of Combinational Logic • Review of Combinational Logic ○ Introduction, Boolean algebra, Algebraic simplification, K-Map, Flip-Flops (FF)& Latches, Mealy and Moore Machines, Equivalent states &reduction of state tables, Sequential circuit timing.	
		Midterm I	
wk 6, 7, 8, 9, 10	**Verilog HDL Models and Synthesis**		
		Description of combinational circuits, modules, assignments, procedural assignments, modeling FF using always blocks, Event control statements, compilation, simulation and synthesis of Verilog codes, Multiplexers..	

wk 11, 12	**Timing Analysis and Optimizations**	
	Midterm II	
wk 13, 14	**Synthesis and Optimizations** **Power Analysis and Optimizations**	
wk 15 & 16	**Review & Project presentation**	
	Final Exam Date: Wednesday, December 13 1715-1930	