San José State University, College of Engineering,
Electrical Engineering Department,
EE270, Advanced Logic Design, Spring 2018

Instructor:	John (JeongHee) Kim
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Office Hours:	M & W 7:20 to 8:30 pm
Class Days/Time:	M & W 4:30 to 5:45 pm
Classroom:	Engr Bldg 401
Prerequisites:	EE118: Logic Design, or equivalent

EE270 Website

Course materials such as the syllabus, major assignment, handouts, etc. may be found on my web page at [https://groups.yahoo.com/groups/SJSU-EE270]. You are responsible for regular checking of the web site.

Course Description

This course presents principles and techniques in logic design: design and analysis of combinational logic circuit; flip-flop properties, sequential circuit analysis and synthesis, algorithmic state machines; asynchronous circuit design and analysis; and design for testability.

The students are required to do exercises and a design project in the open laboratory using HDL-based methodology. The course is intended for senior students and beginning graduate student in the digital design concentration.

Course Learning Objectives:

1. The ability to understand fundamental concepts of synchronous circuit design
2. The ability to perform simplification of switching functions

3. The ability to analyze and synthesize synchronous circuits
4. The ability to understand the classification of asynchronous circuit.
5. The ability to analyze and synthesis fundamental asynchronous circuit design
6. The ability to use HDL for modeling and verification purposes
7. The ability design and test certain class of synchronous and asynchronous circuits
8. The ability to understand fundamental concepts and practices of DFT

Required & Recommended Texts/Software

Text:

1. Digital Logic Circuit Analysis and Design, V. P. Nelson, H. T. Nagle, B. D. Carroll, J. D. Irwin, H Prentice Hall 1995
2. Asynchronous Circuit Design, Chris J. Myers, Prentice Hall 2001
3. Digital Principles and Design, Donald Givone, McGrawHill 2003
2. Contemporary Logic Design, Randy h. Katz and Gaetano Borriello, Prentice Hall 2005

Dropping and Adding

Students are responsible for understanding the policies and procedures about add/drop, grade forgiveness, etc. Refer to the current semester's Catalog Policies section at http://info.sjsu.edu/static/catalog/policies.html. Add/drop deadlines can be found on the current academic calendar web page located at http://www.sjsu.edu/academic_programs/calendars/academic_calendar/. The Late Drop Policy is available at http://www.sjsu.edu/aars/policies/latedrops/policy/**.** Students should be aware of the current deadlines and penalties for dropping classes.

Information about the latest changes and news is available at the Advising Hub at http://www.sjsu.edu/advising/.

Assignments and Grading Policy

Grading:	Homework, attendance & Quiz	15%
	Midterm Exam #1:	20%
	Midterm Exam #2:	20%
	Project presentation & Report	15%
	Final Exam:	30%

Assignments and Grading Policy

Notes on Evaluation:

1. **If you turn in assignments late, maximum of 10% credits** will be given. Solutions to the homework assignments and all other info are posted in group site ([https://groups.yahoo.com/groups/SJSU-EE270]). Everyone must join in this site to get necessary info (Exam sol, Qz sol, HW assignments & sol, and other announcements).

2. **If 75% of combined HW, quizzes, & attendance are not done by end of semester, you will get F grade automatically.**

3. HW has to have cover page given in the group site otherwise you will not get any credits or deducted up to 100 percent. Final solutions on HW and exam must be boxed. Otherwise you will not get credits. Only one side of page must be used in the HWs. (No HW sending through an email will be accepted.) HW should be clean, legible, stapled on top left corner and proper paper should be used.

4. All exams are closed book and note. Only one 8.5 x 11 cheat sheet (both pages) is allowed for each exam (2 midterm exams). You can bring all three cheat sheets in the final exam (2 cheat sheet for the final exam).

5. **No make-up exams (no excuse will be accepted-that is why you get one extra exam), quizzes, HW (no acceptance through an email), Attendance at all. No incomplete grades will be given**. HW must be turned in on a given date only, otherwise it will not be accepted. Most likely, one quiz will be given once a week.

6. **If unreasonable or out of common sense behavior happens in the class, one will be asked to leave from the class and will be given "F" grade.** (No feet on a table or chair, taking hat off, no cellphone use or web surfing, no talking with neighbors). And I will drop you from the class if the class is disturbed unreasonably with my right.

7. **Attendance will be checked randomly (will be considered as one HW)** and will be counted as part of HW & Qz grading.

8. **No food** is allowed (Water is ok). It is mandatory to have a scientific calculator by within two weeks of semester and you need to carry it all the time. All the exams and quizzes are done in the class and only allowed to use pencil and eraser (no pen)

9. If there are any cheatings, all will be reported to the department.

Exams & Term Project:
All exams are in-class. One 8.5x11 front & back summary sheets *in your own handwriting* are allowed. No other photocopied problem solutions or any other course material is allowed.

Open Laboratory:
E 289, E291/Unix-based and E 389/PC-based

Numerical Grade to Letter Grade Conversion:

95% and above	A+,
90-94%	A
86-89%	A-
82-85%	B+
78-81%	B
74-77%	B-
70-73%	C+
66-69%	C
62-65%	C-
58-61%	D+
54-57%	D
50-53%	D-
below 50%	F

University Policies

Academic integrity

Your commitment as a student to learning is evidenced by your enrollment at San Jose State University. The University's Academic Integrity policy, located at http://www.sjsu.edu/senate/S07-2.htm, requires you to be honest in all your academic course work. Faculty members are required to report all infractions to the office of Student Conduct and Ethical Development. The Student Conduct and Ethical Development website is available at http://www.sa.sjsu.edu/judicial_affairs/index.html.

Instances of academic dishonesty will not be tolerated. Cheating on exams or plagiarism (presenting the work of another as your own, or the use of another person's ideas without giving proper credit) will result in a failing grade and sanctions by the University. For this class, all assignments are to be completed by the individual student unless otherwise specified. If you would like to include your assignment or any material you have submitted, or plan to submit for another class, please note that SJSU's Academic Policy S07-2 requires approval of instructors.

Campus Policy in Compliance with the American Disabilities Act

If you need course adaptations or accommodations because of a disability, or if you need to make special arrangements in case the building must be evacuated, please make an appointment with me as soon as possible, or see me during office hours. Presidential Directive 97-03 requires that students with disabilities requesting accommodations must register with the Disability Resource Center (DRC) at http://www.drc.sjsu.edu/ to establish a record of their disability.

EE Department Honor Code

The Electrical Engineering Department will enforce the following Honor Code that must be read and accepted by all students.

"I have read the Honor Code and agree with its provisions. My continued enrollment in this course constitutes full acceptance of this code. I will NOT:

- Take an exam in place of someone else, or have someone take an exam in my place
- Give information or receive information from another person during an exam
- Use more reference material during an exam than is allowed by the instructor
- Obtain a copy of an exam prior to the time it is given
- Alter an exam after it has been graded and then return it to the instructor for re-grading
- Leave the exam room without returning the exam to the instructor."

Measures Dealing with Occurrences of Cheating

- Department policy mandates that the student or students involved in cheating will receive an "F" on that evaluation instrument (paper, exam, project, homework, etc.) and will be reported to the Department and the University.
- A student's second offense in any course will result in a Department recommendation of suspension from the University.

Tentative Class Schedule (will be updated as needed)		
Week	**Topic**	
wk 1 & 2	**Introduction**	
	Review of switching algebra	
	Analysis and synthesis of combinational logic	
	Synchronous vs asynchronous circuits	
	HDL tools	
wk 3 & 4	**Simplification of switching functions [Week 3 and 4]**	
	Karnaugh Maps	
	Quine-McCluskey method	
	Espresso Algorithm	
wk 5, 6 ,7, 8, 9	**Synchronous circuit design [Week 5, 6, 7, 8, 9]**	
	Sequential devices	
	Analysis and synthesis of synchronous sequential circuits	
	Simplification and Optimization of Sequential Circuit	
wk 10, 11, 12, 13	**Asynchronous sequential circuits [Week 10, 11, 12,13]**	
	Huffman Circuit	
	Muller Circuit	
	Timed Circuit	
	Petri-net and Graph-based Methods	
	Transformation Methods	
	Asynchronous data path (pipelines)	
	Verification	
wk 14 & 15	**Introduction to design for testability [Week 14,15]**	
	Fault models	
	Combinational circuit testing	
	Sequential logic circuit	
	DFT	
	Final Exam Date & Time: Wednesday, May 16 1445-1700	