San José State University
Department of Electrical Engineering

Course Title: **Advanced Logic Design**

Meeting:

MW **16:30 - 17:45, E232**
Lab **Open Lab, E389/E291**

Instructor:

Dr. Tri Caohuu, ENG 375
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(408) 924 3951

Office Hours: **MW 17:00 to 18:00**

Course Description:

This course presents principles and techniques in logic design: design and analysis of combinational logic circuit; flip-flop properties, sequential circuit analysis and synthesis, algorithmic state machines; asynchronous circuit design and analysis; and design for testability.

The students are required to do exercises and a design projects in the open laboratory using HDL-based methodology. The course is intended for senior students and beginning graduate student in the digital design concentration.

Text & Ref. Text:

1. *Digital Logic Circuit Analysis and Design,
   V. P. Nelson, H. T. Nagle, B. D. Carroll, J. D. Irwin, H Prentice Hall 1995
2. Asynchronous Circuit Design, Chris J. Myers, Prentice Hall 2001
3. Digital Principles and Design, Donald Givone, McGrawHill 2003
2. Contemporary Logic Design, Randy h. Katz and Gaetano Borriello, Prentice Hall 2005

Grading policy:

Homework	10%
Midterm	25%
Projects	25%
Final Exam	40%

Failure to complete and submit 80% of homework and project assignments will result in a failing grade in this class.

Grading Grade	Overall Score
A+	95-100
A	90-94
B+	85-89
B	80-84
C+	75-79
C	70-74
D+	65-69
D	60-64
F	0-59

Late Penalty
No late assignments will be accepted

Makeup Exam
No makeup exams will be given unless you have documented compelling reasons.

COURSE OUTLINE

I. Introduction
- Review of switching algebra
- HDL tools

II. Simplification of switching functions
- Quine-McCluskey method
- Espresso Algorithm

III. Synchronous circuit design
- Sequential devices
- Analysis and synthesis of synchronous sequential circuits
- Simplification and optimization of sequential Circuit

IV. Asynchronous sequential circuits
- Huffman Circuit
- Muller Circuit
- Petri-net and Graph-based Methods
- Asynchronous data path (pipelines)

V. Introduction to design for testability
- Fault models
- Combinational circuit testing
- Sequential logic circuit
- Design For Testability

VI. Design Project

Final Exam :	Wednesday, Dec 13, 2015	14:45-17:00

TENTATIVE SCHEDULE

Week	Date	Topics	Homework	Laboratory
1	8/23	Introduction		
2	8/28,30	Review of Boolean Algebra		
3	9/4	Labor Day		
	9/6	Review of Boolean Algebra	1	
4	9/11,13	Introduction to VHDL		
5	9/18,20	VHDL	2	
6	9/25	Quine-McCluskey method		
	9/27	Espresso Algorithm	3	
7	10/2	Espresso Algorithm		
	10/4	Sequential Devices		
8	10/9,11	Analysis & Synthesis of Synchronous Sequential Circuit	4	
9	10/16,18	Simplification and Optimization Of Sync. Seq. Circuit		
10	10/23,25	Review & MIDTERM		Project
11	10/30	Async. Circuit (Huffman)	5	
	11/1	Async. Circuit (Huffman) cont.		
12	11/6,8	Asynchronous Circuit (Muller)	6	
13	11/13,15	Asynchronous Circuit (Muller)		
14	11/20,22	Async. Pipelines		
15	11/27,29	Design for Testability	7	
16	12/4,6	Design for Testability		
17	12/11	Review for Final		
	12/13	FINAL EXAM		

Course Learning Objectives:

1. The ability to understand fundamental concepts of synchronous circuit design
2. The ability to perform simplification of switching functions
3. The ability to analyze and synthesize synchronous circuits
4. The ability to understand the classification of asynchronous circuit.
5. The ability to analyze and synthesis fundamental asynchronous circuit design

6. The ability to use HDL for modeling and verification purposes

7. The ability design and test certain class of synchronous and asynchronous circuits

8. The ability to understand fundamental concepts and practices of DFT

University, College, or Department Policy Information

a) Academic integrity statement (from Office of Judicial Affairs):
"Your own commitment to learning, as evidenced by your enrollment at San José State University and the University's Academic Integrity Policy requires you to be honest in all your academic course work. Faculty are required to report all infractions to the Office of Judicial Affairs. The policy on academic integrity can be found at http://www2.sjsu.edu/senate/S04-12.pdf

b) Campus policy in compliance with the Americans with Disabilities Act:
"If you need course adaptations or accommodations because of a disability, or if you need special arrangements in case the building must be evacuated, please make an appointment with me as soon as possible, or see me during office hours. Presidential Directive 97-03 requires that students with disabilities register with DRC to establish a record of their disability."

c) Cell Phones: Students will turn their cell phones off or put them on vibrate mode while in class. They will not answer their phones in class. Students whose phones disrupt the course and do not stop when requested by the instructor will be referred to the Judicial Affairs Officer of the University.

d) Academic Honesty: Faculty will make every reasonable effort to foster honest academic conduct in their courses. They will secure examinations and their answers so that students cannot have prior access to them and proctor examinations to prevent students from copying or exchanging information. They will be on the alert for plagiarism. Faculty will provide additional information, ideally on the green sheet, about other unacceptable procedures in class work and examinations. Students who are caught cheating will be reported to the Judicial Affairs Officer of the University, as prescribed by Academic Senate Policy S04-12.

EE Department Honor Code

The Electrical Engineering Department will enforce the following Honor Code that must be read and accepted by all students.

"I have read the Honor Code and agree with its provisions. My continued enrollment in this course constitutes full acceptance of this code. I will NOT:

- Take an exam in place of someone else, or have someone take an exam in my place
- Give information or receive information from another person during an exam
- Use more reference material during an exam than is allowed by the instructor
- Obtain a copy of an exam prior to the time it is given
- Alter an exam after it has been graded and then return it to the instructor for re-grading

- Leave the exam room without returning the exam to the instructor."

Measures Dealing with Occurrences of Cheating

- Department policy mandates that the student or students involved in cheating will receive an "F" on that evaluation instrument (paper, exam, project, homework, etc.) and will be reported to the Department and the University.
- A student's second offense in any course will result in a Department recommendation of suspension from the University.

APPENDIX:

• "You are responsible for understanding the policies and procedures about add/drops, academic renewal, withdrawal, etc. found at http://www2.sjsu.edu/senate/S04-12.pdf

• Expectations about classroom behavior; see Academic Senate Policy S90-5 on Student Rights and Responsibilities.

• As appropriate to your particular class, a definition of plagiarism, such as that found on Judicial Affairs website at http://www2.sjsu.edu/senate/plagarismpolicies.htm

• "If you would like to include in your paper any material you have submitted, or plan to submit, for another class, please note that SJSU's Academic Integrity policy S04-12 requires approval by instructors."