San José State University
Department of Electrical Engineering
EE230, RFIC Design II, Spring, 2017

Course and Contact Information

Instructor: Dr. Marshall Wang

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Office Hours: MW 7:15pm – 7:45pm

Class Days/Time: MW 6:00pm – 7:15pm

Classroom: Clark Building 117

Prerequisites: EE220 or Instructor consent

Course Description

This course is a design/hands-on intensive overview of low noise amplifiers, conventional and switching power amplifiers, LC and voltage controlled oscillators, mixers, phase shifters, attenuators with advanced layout techniques and analytic skills to improve the noise, linearity, stability, efficiency and bandwidth of communication circuits realized using nano-scale CMOS technologies.

Course Learning Outcomes (CLO)

- The ability to design and analyze high speed LC and voltage controlled oscillator circuits
- The ability to understand and design the characteristics of passive and active Mixer circuits
- The ability to analyze Gilbert cell and translinear circuits
- The ability to understand filtering theory and design of poly phase filters
- The ability to analyze frequency instability caused by circuit parasitics or architecture
- The ability to learn methods and simulation tools to characterize complex RF integrated circuits
- The ability to calculate the thermal, shot and flicker noise and design low noise amplifiers
- The ability to understand the RF signal components and their impact on power and bandwidth
- The ability to determine the trade-off among linearity, efficiency and output power of amplifiers
- The ability to perform team work and analyze the operation of wireless transmitters and receivers

Required Texts/Readings

Textbook

- B. Razavi, RF Microelectronics, 2nd Edition, Upper Saddle River, New Jersey, Prentice Hall, 2012.

Other Readings

- T. H. Lee, The Design of CMOS Radio Frequency Integrated Circuits, Cambridge, U.K., Cambridge University Press, 2004.
- D.M. Pozar, Microwave Engineering, New York, John Wiley, 2004.
- Selected publications from journal of solid-state circuits (JSSC), transactions on microwave theory and techniques (MTT), international solid-state circuit conference (ISSCC) and custom integrated circuits conference (CICC). Papers can be downloaded from IEEE xplore website.

Course Requirements and Assignments

SJSU classes are designed such that in order to be successful, it is expected that students will spend a minimum of forty-five hours for each unit of credit (normally three hours per unit per week), including preparing for class, participating in course activities, completing assignments, and so on. More details about student workload can be found in University Policy S12-3 at http://www.sjsu.edu/senate/docs/S12-3.pdf.

Final Examination or Evaluation

Exams:
The dates of exams are shown on the course syllabus. There will be no make-up exam and those absent will receive no credit. Students must write their answers clearly in an organized fashion. Further instructions will be provided during exams.

Design Project:

Projects are mainly based on Cadence and are closely related to topics discussed in this course.
Cadence will not be taught in this course and students are required to master this CAD tool by themselves. More details on projects, related to the topics discussed in this course, will be provided as the lectures progress. Projects, assigned to different student groups (maximum 2 students per group), require a formal report typed using Microsoft Office word processor with all original figures included. Students must submit the printed version of their reports along with all supporting data, circuits, graphs and the report soft copy, as a *.tar.gz file, in a readable CD and as an attachment to an email before deadline.

NOTE that University policy F69-24 at http://www.sjsu.edu/senate/docs/F69-24.pdf states that “Students should attend all meetings of their classes, not only because they are responsible for material discussed therein, but because active participation is frequently essential to insure maximum benefit for all members of the class. Attendance per se shall not be used as a criterion for grading.”

Grading Information

Mid-term Exam	35%
Final Exam	45%
Individual Design Project	20%

Determination of Grade

100% - 90%	A	71.9% - 69%	C
89.9% - 85%	A-	68.9% - 65%	C-
84.9% - 82%	B+	64.9% - 62%	D+
81.9% - 79%	B	61.9% - 59%	D
78.9% - 75%	B-	58.9% - 55%	D-
74.9% - 72%	C+	54.9% and below	F

Classroom Protocol

1. Attend all class meetings on time
2. Focus in the lecture without private conversation and cell phone communication
3. Treat all in class with respect

University Policies

Per University Policy S16-9, university-wide policy information relevant to all courses, such as academic integrity, accommodations, etc. will be available on Office of Graduate and Undergraduate Programs' Syllabus Information web page at http://www.sjsu.edu/gup/syllabusinfo/"

EE230 / RFIC Design II, Spring 2017, Course Schedule

Course Schedule

Week	Date	Topics, Readings, Assignments, Deadlines
1	1/30	RFIC Introduction and Nonlinearity
1	2/1	Wireless Receiver Architecture - I
2	2/6	Wireless Receiver Architecture - II
2	2/8	Common-Source LNA with Inductive Load
3	2/13	Common-Source LNA with Resistive Feedback
3	2/15	Common Gate LNA with Ro effect
4	2/20	Cascode Common-Gate LNA
4	2/22	Cascode Common-Source LNA
5	2/27	Common-Source LNA with Source Degeneration
5	3/1	Wireless Transmitter Architecture - I
6	3/6	Wireless Transmitter Architecture - II
6	3/8	Power Amplifier Considerations
7	3/13	Power Amplifier – Class A, B, AB
7	3/15	Power Amplifier – Class C, E, F,
8	3/20	Midterm Exam Review
8	3/22	Midterm Exam
9	3/27	Spring Recess
9	3/29	Spring Recess
10	4/3	Oscillator Key Design Parameters
10	4/5	Oscillator Principles
11	4/10	Cross Coupled Oscillator
11	4/12	Voltage Controlled Oscillator
12	4/17	LC VCO with Wide Tuning Range, Varactors
12	4/19	Mixer Considerations
13	4/24	Passive Down-Conversion Mixer – single/double balanced
13	4/26	Passive Down-Conversion Mixer – Gain and NF
14	5/1	Active Mixer Principles
14	5/3	Active Mixer Principles – Gain and NF
15	5/8	RFIC Product Development Procedure
15	5/10	Final Exam Review

Week	Date	Topics, Readings, Assignments, Deadlines
16	5/15	Study/Conference Day – no class or exams
Final Exam	5/22	Project Due by Midnight