SAN JOSE STATE UNIVERSITY
COLLEGE OF ENGINEERING
DEPARTMENT OF ELECTRICAL ENGINEERING

EE 224-01, High Speed CMOS Circuits Fall 2017

Instructor:	Khosrow Ghadiri
Office Location:	ENGR 255
Telephone:	(408) 924-3916
Fax:	(408) 924-3925
Email:	k.ghadiri@sjsu.edu
Website URL:	TBA
Office Hours:	MW 17:00-18:00 TR 15:30-16:30
Class Days/Time:	MW 19:30-20:45
Classroom:	ENGR. 403
Prerequisites:	EE 221, Basic knowledge of transistor modeling, digital and analog circuit

Course Description

High speed CMOS design concept beyond traditional static CMOS. High speed transistor level logic design, with various modules used as design examples. Overall concepts will be tied together by a design project. Team work will be stressed.

Specific topics covered in EE 224 include:

1- Analyze CMOS and diode circuit in large signal domain.
2- Understanding of the concept CMOS digital circuit such as inverter…
3- Design and size combinational CMOS logic..
4- Design and size sequential CMOS circuit.
5- Use modern engineering CAD tools
6- Verify the theory with hands-on lab simulation

Course Goals and Student Learning Objectives (LO):

LO1: Understanding MOSFET and Diode circuit in large scale signal domain.
LO2: Understanding transistor sizing for high speed logic design gates.
LO3: The ability to size transistors for high speed low power combinational logic.
LO4: The ability to size transistors for high speed low power sequential circuits.
LO5 Understanding the concept of buffer design.
LO6: Understanding the concept of logical effort design.
LO7: The ability to run transistor level circuit simulation.

Required Textbook:

Digital Integrated Circuit, Jan Rabaey, Prentice Hall, 2nd edition

Recommended Texts

CMOS VLSI, N. Weste & D. M. Harris
Low Power Digital VLAI Design Circuit and Systems, Abdellatouar, Mohamed Elmasry 1995 XVII p530
Analysis and Design of Digital Integrated Circuits: In Deep Sub micron Technology, D. A. Hodges, H. G. Jackson, and R. A. Saleh, 3rd edition McGraw-Hill series in Electrical Engineering, Vol. 3118 Boston, MA.

Software:

Cadence, available for student at Cadence open lab.

Other Readings

Handouts either posted on the web page or distributed in class.

Classroom Protocol

Students will turn their cell phones off or put them on vibrate mode while in class. They will not answer their phones in class. Students whose phones disrupt the course and do not stop when requested by the instructor will be referred to the Judicial Affairs Officer of the University**.**

Assignments and Grading Policy

Homework

Homework assignments represent a minimum number of suggested practice problems for the students to solve for the purposes of testing their understanding of the material covered in lecture. Homework assignments will be picked up or graded. They should be treated as an invaluable tool for getting a good grasp of the material covered in this course. Working out additional appropriate problems available to the student for practice purposes is highly recommended. Its relationship to exams is like batting practice before a baseball game.

Projects

Projects are mainly based on circuit implementation in Cadence and are closely related to topics discussed in this course. Cadence will not be taught in this course and students are required to master this CAD tools by themselves. However the Cadence tutorial will be available to students. Each group (maximum of four students) must write a formal project report using a word processor (i.e. Microsoft Office,…) and submit the original write up including all data, images and graphs in a CD and by email or memory stick before deadline to be eligible to receive a credit. Students may be required to present their works similar to standard design review as conducted in industry. More detail on design projects will be provided as a lectures progress.

Course Grading

Letter grade will be assigned based on the distribution curves for each exam. Using the following schedule of weights, the weighted sum of these numerical scores (rounded to the nearest integer) will be used to determine the course grade:

97% and above	A+
94% - 96%	A
90% - 93%	A-
87% - 89%	B+
83% - 86%	B
80% - 82%	B-
77% - 79%	C+

73% - 76%	C
70% - 72%	C-
67% - 69%	D+
63% - 66%	D
60% - 62%	D-
Below 59%	F

Using the following schedule of weights, the weighted sum of these numerical scores (rounded to the nearest integer) will be used to determine the course grade:

Homework	5%
Exam 1	15%
Exam 2	15%)
Design Project	30%
Final exam	35%
Total	100%

Note that except for extraordinary, documented situations, make-up exams will not be allowed. Thus, at the beginning of the semester make sure that you have no exam conflicts. Students having disabilities, which require special exam conditions are urged to consult the Disabled Students Office immediately and are asked to inform the instructor of any special needs

Classroom Protocol

Students are expected to participate actively in class. Students will turn their cell phones off or put them on vibrate mode while in class. They will not answer their phones in class.

Dropping and Adding

Students are responsible for understanding the policies and procedures about add/drop, grade forgiveness, etc. Refer to the current semester's Catalog Policies section at http://info.sjsu.edu/static/catalog/policies.html. Add/drop deadlines can be found on the current academic calendar web page at http://www.sjsu.edu/provost/Academic_Calendars/. The Late Drop Policy is available at http://www.sjsu.edu/aars/policies/latedrops/policy/**.** Students should be aware of the current deadlines and penalties for dropping classes.

Information about the latest changes and news is available at the Advising Hub at http://www.sjsu.edu/advising/.

University Policies

Academic integrity

Your commitment as a student to learning is evidenced by your enrollment at San Jose State University. The University's Academic Integrity policy, located at http://www.sjsu.edu/senate/S07-2.htm, requires you to be honest in all your academic course work. Faculty members are required to report all infractions to the office of Student Conduct and Ethical Development. The Student Conduct and Ethical Development website is available at http://www.sjsu.edu/studentconduct/.
Instances of academic dishonesty will not be tolerated. Cheating on exams or plagiarism (presenting the work of another as your own, or the use of another person's ideas without giving proper credit) will result in a failing grade and sanctions by the University. For this class, all assignments are to be completed by the individual student unless otherwise specified. If you would like to include your assignment or any material you have submitted, or plan to submit for another class, please note that SJSU's Academic Integrity Policy S07-2 requires approval of instructors.

Campus Policy in Compliance with the American Disabilities Act

If you need course adaptations or accommodations because of a disability, or if you need to make special arrangements in case the building must be evacuated, please make an appointment with me as soon as possible, or see me during office hours. Presidential Directive 97-03 at http://www.sjsu.edu/president/docs/directives/PD_1997-03.pdf requires that students with disabilities requesting accommodations must register with the Disability Resource Center (DRC) at http://www.drc.sjsu.edu/ to establish a record of their disability.

EE Department Honor Code

The Electrical Engineering Department will enforce the following Honor Code that must be read and accepted by all students.

"I have read the Honor Code and agree with its provisions. My continued enrollment in this course constitutes full acceptance of this code. I will NOT:

- Take an exam in place of someone else, or have someone take an exam in my place
- Give information or receive information from another person during an exam
- Use more reference material during an exam than is allowed by the instructor
- Obtain a copy of an exam prior to the time it is given
- Alter an exam after it has been graded and then return it to the instructor for re-grading
- Leave the exam room without returning the exam to the instructor."

Measures Dealing with Occurrences of Cheating

Department policy mandates that the student or students involved in cheating will receive an "F" on that evaluation instrument (paper, exam, project, homework, etc.) and will be reported to the Department and the University. A student's second offense in any course will result in a Department recommendation of suspension from the University.

Schedule

WEEK	DATE	TOPICS	READING
1	Wed. 08/23/17	IC resistors	
2	Mon. 08/28/17	Diode in large signal domain-1	
	Wed. 08/30/17	Diode in large signal domain-2, Small signal & dynamic behavior	
3	**Mon. 09/04/17**	**Labor Day**	
	Wed. 09/06/17	MOSFET in large signal domain-1	
4	Mon. 09/11/17	MOSFET in large signal domain-2	
	Wed. 09/13/17	CMOS inverter-1	
5	Mon. 09/18/17	CMOS inverter-2	
	Wed. 09/20/17	CMOS inverter-3	
6	Mon. 09/25/17	**Midterm 1**	
	Wed. 09/27/17	CMOS inverter-4	
7	Mon. 10/02/17	Buffer Design-1	
	Wed. 10/04/17	Buffer Design-2	
8	Mon. 10/09/17	Combinational logic-1	
	Wed. 10/11/17	Combinational logic-2	
9	Mon. 10/16/17	Combinational logic-3	
	Wed. 10/18/17	Combinational logic-4	
10	Mon. 10/23/17	Logical Effort-1	
	Wed. 10/25/17	Logical Effort-2	
11	**Mon. 10/30/17**	**EXAM II**	
	Wed. 11/01/17	Sequential circuits-2	
12	Mon. 11/06/17	Sequential circuits-3	
	Wed. 11/08/17	Sequential circuits-4	
13	Mon. 11/13/17	Sequential circuits-5	
	Wed. 11/15/17	Sequential circuits-6	
14	Mon. 11/20/17	Advanced topics and futures-1	
	Wed. 11/22/17	Advanced topics and futures-2	
15	Mon. 11/27/17	Advanced topics and futures-1	
	Wed. 11/29/17	Project demo and presentation 1	
16	Mon. 12/04/17	Project demo and presentation-2	
	Wed. 12/06/17	Review	
	Wed. 12/13/17	**COMPREHENSIVE FINAL EXAM 19:45-22:00**	