San José State University
Department of Electrical Engineering
EE223, Analog Integrated Circuits
Number 45885, Section 01, Fall 2017

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Office Hours: Tuesdays/Thursdays 17:50 to 18:50, Other time by appointment
Class Schedule: Tuesdays/Thursdays 16:30-17:45
Classroom: ENGR401
Prerequisites: Graduate Standing

Course Description:

This course studies nanoscale metal-oxide semiconductor field effect transistor (MOSFET) modeling and circuit design techniques for analog integrated circuit applications. Course topics include short channel issues, layout techniques to improve design performance, noise modeling and transformation, wide-swing current mirrors, gain, bandwidth and voltage swing characteristics of single-stage and two-stage amplifiers. A variety of opamp architectures including fully-differential structures with their slew rate, settling time, phase margin, stability, gain and bandwidth will be discussed in detail. Finally, the application of the fully-differential opamp in switched-capacitor circuits is discussed for a class project. The class project will be designing a pipeline stage consisted of a sub-ADC using clocked comparators, DAC logic, a multiplying DAC, clock and reference circuits based on a CMOS bandgap.

Required Textbook:

- Design of Analog CMOS Integrated Circuits, by Behzad Razavi, McGraw-Hill, 2001.

Other Reference Materials:

- Analog Integrated Circuit Design, 2nd Edition, by Tony Chan Carusone, David A. Johns and Ken Martin, Wiley, 2011. http://analogicdesign.com
- CMOS Circuit Design, Layout, and Simulation, 3rd Edition, by R. Jacob Baker, IEEE Press, Wiley, 2010.
- Analysis and Design of Analog Integrated Circuits, 5th Edition, by Gray, Hurst, Lewis and Meyer, Wiley, 2009.

Grading:

assignments	25%
midterm exam	25%
design project	25%
final exam	25%

Grading Percentage Breakdown:

90% and above	A
89% - 85%	A-
84% - 82%	B+
81% - 79%	B
78% - 75%	B-
74% - 72%	C+
71% - 69%	C
68% - 65%	C-
64% - 62%	D+
61% - 59%	D
58% - 55%	D-
below 55%	F

Exams:

The date of the exams is shown on the course syllabus. Exams will be closed book. However, students are allowed to bring 1 page of aid sheet. There will be no make-up exam and those absent will receive no credit. Students must write their answers clearly in an organized fashion. Further instructions will be provided during exams.

Projects:

Assignments and projects are mainly based on Cadence and are closely related to topics discussed in this course. Cadence will not be taught in this course and students are required to master this CAD tool by themselves. Each group (maximum 4 students) must write a formal project report using a word processor (i.e. Microsoft Office) and submit the original write-up including all data, images and graphs by email before deadline to be eligible to receive a credit. Students may be required to present their works similar to standard design reviews as conducted in industry. Non-restricted MOSFET transistor models will be provided for assignments and projects. More details on design projects will be provided as the lectures progress.

Academic Integrity Statement:

Your own commitment to learning, as evidenced by your enrollment at San Jose State University, and the University's Academic Integrity Policy requires you to be honest in all your academic course work. Faculty members are required to report all infraction to the Office of Student Conduct and Ethical Development. The policy on academic integrity can be found at http://sa.sjsu.edu/student_conduct

Students in this course are expected to maintain high ethical standards in all matters pertaining to the course, including, but not limited to, examinations, homework, course assignments, presentations, writing, laboratory work, team work, treatment of class members, and behavior in class. Cheating and plagiarism are violations of the SJSU Policy on Academic Dishonesty (S98-1) and will not be tolerated in the class. Students are expected to have read the Policy, which is available at http://www2.sjsu.edu/senate/S014-12.pdf

Campus Policy in Compliance with the Americans with Disabilities Act:

If you need course adaptations or accommodations because of a disability, if you have emergency medical information to share or if you need to make special arrangements in case the building must be evacuated, please make an appointment with your course instructor or see him/her during office hours as soon as possible.

Course Goals:

1. Students will be able to design advanced biasing circuits, opamps, comparators and switch-capacitor circuits.
2. Students will be able to understand the concept of noise, distortion, stability, phase margin, voltage swing, slew-rate and gain-bandwidth product.
3. Students will be able to use modern engineering CAD tools for computations, simulations, analysis, and design.
4. Students will be able to verify the theory with hands-on lab simulations.

Course Learning Objectives:

- The ability to characterize and model transistors
- The ability to bias and operate transistors as amplifiers
- The ability to design amplifiers with different characteristics
- The ability to design high performance layout with minimum parasitics
- The ability to utilize simulation tools to characterize complex Analog integrated circuits
- The ability to determine the trade-off among linearity, bandwidth, gain and power dissipation of amplifiers
- The ability to design stable multi-stage amplifiers
- The ability to apply frequency compensation techniques for amplifiers
- The ability to design temperature and supply independent bandgap reference circuits
- The ability to design clocked comparator for ADC application
- The ability to design 2-phase clock and switched-capacitor circuits for ADC application

*Tentative Course Syllabus and Schedule**

Date	Topics	Book reading
24-Aug	Introduction to Analog IC design, Project Description 1	Chapter 1
29-Aug	MOS Device Physics 1	Chapter 2
31-Aug	MOS Device Physics 2 (**HW#1 handout**)	Chapter 2
5-Sep	Single Stage Amplifiers 1	Chapter 3
7-Sep	Single Stage Amplifiers 2	Chapter 3
12-Sep	Differential Amplifiers	Chapter 4
14-Sep	Current Mirrors (**HW#2 handout, HW#1 due, 5% grade**)	Chapter 5
19-Sep	Frequency Response 1	Chapter 6
21-Sep	Frequency Response 2	Chapter 6
26-Sep	Noise – Flicker and Thermal	Chapter 7
28-Sep	Noise in Amplifiers (**HW#3 handout, HW#2 due, 5% grade**)	Chapter 7
3-Oct	Feedback 1	Chapter 8
5-Oct	Feedback 2	Chapter 8
10-Oct	OPAMP - Single Stage	Chapter 9
12-Oct	OPAMP - Two Stage, Gain Boosting (**HW#4 handout, HW#3 due, 5% grade**)	Chapter 9
17-Oct	Stability and Frequency Compensation	Chapter 10
19-Oct	***Midterm Exam, 75 minutes, 25% grade***	
24-Oct	Fully differential OPAMP	Lecture note
26-Oct	Common-Mode Feed-Back (CMFB)	Lecture note
31-Oct	Bandgap reference	Chapter 11
2-Nov	Switched-Capacitor Circuits (**HW#5 handout, HW#4 due, 5% grade**)	Chapter 12
7-Nov	Sample & Hold and MDAC	Lecture note
9-Nov	Comparators and Clock Circuits	Lecture note
14-Nov	Project Description 2	Lecture note
16-Nov	Nonlinearity, Mismatch, Offset Cancellation (**HW#5 due, 5% grade**)	Chapter 13
21-Nov	Analog Layout Techniques	Chapter 18
23-Nov	Thanksgiving Holiday - No Class	
28-Nov	Project Presentation - Group A, B	
30-Nov	Project Presentation - Group C, D	
5-Dec	Project Presentation - Group E, F	
7-Dec	Review for Final Exam	
12-Dec	Study/Conf. Day (**online Project report submission due by noon, 25% grade**)	
13-Dec	***Final Exam, from 14:45 — 17:00, 25% grade***	

Thanksgiving Holiday: 11/23

*Midterm Exam date is approximate and subject to change with reasonable notice.