San José State University
College of Engineering/Electrical Engineering
EE221, Principles of Semiconductor Devices I, Section-04, Fall 2017

Course and Contact Information

Instructor:	**Bhaskar L. Mantha**
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Office Hours:	TTh 3:30-5:30 pm or by appointment (ENG 383)
Class Days/Time:	TTh 6:00-7:15pm
Classroom:	Dudley Moorhead Hall 149B (DMH 149B)
Prerequisites:	EE128 or consent of instructor

Faculty Web Page

Copies of the course materials such as the syllabus, major assignment handouts, your grades, etc. can be found in SJSU/Canvas. You are responsible for regularly checking with the messaging system through MySJSU and your email as shown on class roster. Instructor email: bhaskar.mantha@sjsu.edu

Course Description

This course is a prerequisite for all the electronics courses and reviews semiconductor device physics and technology. The students are expected to have some background in atomic physics and solid state physics for this course. The course is divided into four parts- semiconductor fundamentals, p-n junctions, bipolar junction transistors (BJT), and field effect transistors (FET).

Course Goals and Student Learning Objectives

Upon successful completion of this course, students will be able to:

LO1 **Describe** fundamental concepts of solid-state physics applied to the semiconductor devices by Silicon and compound semiconductor materials.

LO2 **Explain** general electrical behavior of semiconductor Si and GaAs, construct appropriate physical models.

LO3 **Illustrate** structural details and current-voltage characteristics of p-n junction diode, BJT, MOSFET, Metal/semiconductor diode, and MESFET.

LO4 **Apply** the fundamental understandings of semiconductor devices with knowledge on the limitations of physical models.

Required Texts/Readings

Textbook

Semiconductor Devices: Physics and Technology, by S. M. Sze and M. K. Lee, John Wiley, 2012, ISBN 978-0-470-53794-7

EE221 covers most of the contents of Chapters 0-7 of the book.

Other Readings

1. Solid State Electronic Devices, 7th ed., Ben G. Streetman, S.K. Banerjee, Prentice Hall, 2015
2. Physics and Technology of Semiconductor Devices, A.S. Grove, John Wiley, 1967.
3. Semiconductor Devices, S.M. Sze, John Wiley, 1985.
4. Device Electronics for Integrated Circuits, RS. Muller and T.I. Kamins, John Wiley, 1977.
5. VLSI Fabrication Principles, Sorab K. Ghandhi, John Wiley, 1983.
6. VLSI Technology, S.M. Sze, McGraw- Hill, 1985.
7. Microelectronic Processing- An Introduction to Manufacturing Integrated Circuits, W. Scott Ruska, McGraw- Hill, 1987.
8. Electronic Materials Science for Integrated Circuits in Si and GaAs, Shyam P. Murarka and Martin C. Peckerer, Academic Press, 1989.
9. Electronic materials Science and Technology, James W. Mayer and S.S. Lau, Macmillan, 1990.)

Classroom Protocol

Active participation of students is required. Students will turn their cell phones off or put them on vibrate mode while in class. They will not answer their phones in class. They will not engage in conversions among themselves.

Assignments and Grading Policy

a. **Homework**
Homework is assigned and is posted online during the semester (usually one per chapter). Homework will be collected. The solution will be posted in Canvas.

b. **Quiz**
Pop quizzes are given during the semester. It is once a week most of the time.

c. **Exams**
There are two mid-term examinations and one final examination.

d. **Class Participation**:
Class participation is required and student attendance will be checked.

Dropping and Adding

Students are responsible for understanding the policies and procedures about add/drop, grade forgiveness, etc. Add/drop deadlines can be found on the current academic year calendar on the Academic Calendars web page at http://www.sjsu.edu/provost/academic_affairs/resources/academic_calendars/. Students should be aware of the current deadlines and penalties for dropping classes (Late Drop Information at http://www.sjsu.edu/aars/policies/latedrops/policy/).

Grading Policy

Homework	5%
Quizzes & Class participation	10%
Midterm Exams (2)	25% each
Final Exam	35%
Total	**100%**

Final Grade Percentage Breakdown

Above 97%	A+
94% - 97%	A
90% - 93%	A-
80% - 89%	B+
70% - 79%	B
65% - 69%	B-
60% - 64%	C+
55% - 59%	C
50% - 54%	C-
45% - 49%	D+
40% - 44%	D
Below 40%	F

University Policies

Per University Policy S16-9, university-wide policy information relevant to all courses, such as academic integrity, accommodations, etc. will be available on Office of Graduate and Undergraduate Programs' Syllabus Information web page at http://www.sjsu.edu/gup/syllabusinfo/"

Academic integrity

Students should know that the University's Academic Integrity Policy is availabe at http://www.sa.sjsu.edu/download/judicial_affairs/Academic_Integrity_Policy_S07-2.pdf. Your own commitment to learning, as evidenced by your enrollment at San Jose State University and the University's integrity policy, require you to be honest in all your academic course work. Faculty members are required to report all infractions to the office of Student Conduct and Ethical Development. The website for Student Conduct and Ethical Development is available at http://www.sa.sjsu.edu/judicial_affairs/index.html.

Academic dishonesty will not be tolerated. Cheating on exams or plagiarism (presenting the work of another as your own, or the use of another person's ideas without giving proper credit) will result in a failing grade and sanctions by the University. For this class, each student should complete all assignments unless otherwise specified.

If there are more sections of the same course and if the same homework problems are assigned in each section, it is expected that the students in both sections do independent work in order to solve the given problems. There should not be any copying or discussions between students in a given section or from different sections.

EE221/Principles of Semiconductor Devices, Section-4
Fall 2017, Course Schedule

The schedule is subject to change with fair notice. Will be announced in the class.

week	date	Topic	Reading
1	08/24	Class logistics and Introduction to semiconductor device and technology	Chapter 0
2	08/29, 8/31	Semiconductor materials, energy bands	Chapter 1: 1.1-1.4
3	09/05, 09/07	Intrinsic semiconductor, doping Carrier transport: Drift and diffusion	Chapter 1.5-1.6 Chapter 2: 2.1-2.2
4	09/12, 09/14	Carrier transport: Continuity equation and other processes (generation and recombination)	Chapter 2: 2.3-2.6
5	09/19, 09/21	p-n Junctions fabrication equilibrium conditions	Chapter 3: 3.1-3.2
6	09/26, 09/28	p-n junction operation, junction breakdown, hetero junction	Chapter 3: 3.3-3.7
7	10/03, 10/05	Review for 1st exam, **1st Mid-Exam, 10/05, Thursday, Class room: TBD**	
8	10/10, 10/12	1st exam solutions; Bipolar Transistor Fundamentals: Transistor action, Static charac.	Chapter 4: 4.1-4.2
9	10/17, 10/19	Frequency response and switching of BJT, Heterojunction BJT(HBT)	Chapter 4: 4.3-4.5
10	10/24, 10/26	Ideal MOS-C Capacitor SiO_2-Si MOS Capacitor, Real MOS-C	Chapter 5: 5.1-5.3
12	10/31, 11/02	Review 2nd midterm examination **2nd midterm exam, 11/02, Thursday, Class room: TBD**	
13	11/07, 11/09	2nd mid-exam solutions MOSFET fundamentals	Chapter 5: 5.5
14	11/14, 11/16	Advanced MOSFET: MOSFET Scaling	Chapter 6: 6.1
15	11/21, 11/23	Advanced MOSFET: CMOS & BiCMOS, SOI **11/23 No class – Thanksgiving**	Chapter 6: 6.2, 6.3
16	11/28, 11/30	MS Contacts, MESFET	Chapter 7: 7.1, 7.2
17	12/05, 12/07	MESFET, MODFET **Review for final**	Chapter 7: 7.2,7.3
Final Exam.: Dec. 19, 2017, Tuesday, 5:15 pm-7:30 pm, Class room: TBD			

Spring 2017
San Jose State University
Electrical Engineering Department

EE Department Honor Code

The Electrical Engineering Department will enforce the following Honor Code that must be read and accepted by all students.

"I have read the Honor Code and agree with its provisions. My continued enrollment in this course constitutes full acceptance of this code. I will NOT:

- *Take an exam in place of someone else, or have someone take an exam in my place*
- *Give information or receive information from another person during an exam*
- *Use more reference material during an exam than is allowed by the instructor*
- *Obtain a copy of an exam prior to the time it is given*
- *Alter an exam after it has been graded and then return it to the instructor for re-grading*
- *Leave the exam room without returning the exam to the instructor."*

Measures Dealing with Occurrences of Cheating

- *Department policy mandates that the student or students involved in cheating will receive an "F" on that evaluation instrument (paper, exam, project, homework, etc.) and will be reported to the Department and the University.*
- *A student's second offense in any course will result in a Department recommendation of suspension from the University.*