San José State University
College of Engineering/Electrical Engineering
EE221, Principle of Semiconductor Devices I, Section-01, Fall 2017

Instructor:	**Lili He**
Office Location:	ENG 357
Telephone:	(408) (924-4073)
Email:	lili.he@sjsu.edu
Office Hours:	TR 1:45-2:45pm or by appointment
Class Days/Time:	TR 3:00-4:15pm
Classroom:	ENG 331
Prerequisites:	EE128 or Consent of instructor

Canvas and MYSJSU Messaging

Copies of the course materials such as the syllabus, major assignment handouts, homework solutions, etc. may be found on my faculty web page at SJSU Canvas You are responsible for regularly checking through Canvas and your MySJSU messaging information.

Course Description

This course is a prerequisite for all electronics area courses and reviews semiconductor device physics and technology. The students are expected to have some background in atomic physics and solid state physics for this course. The course is divided into four parts-semiconductor fundamentals, p-n junctions, bipolar junction transistors (BJT), and field effect transistors (FET).

Course Goals and Student Learning Objectives

Upon successful completion of this course, students will be able to:

LO1 **Describe** fundamental concepts of solid-state physics applied to the semiconductor devices by Silicon and compound semiconductor materials.
LO2 **Explain** general electrical behavior of semiconductor Si and GaAs, construct appropriate physical models.
LO3 **Illustrate** structural details and current-voltage characteristics of p-n junction diode, BJT, MOSFET, Metal/semiconductor diode, and MESFET.

LO4 **Apply** the fundamental understandings of semiconductor devices with knowledge on the limitations of physical models.

Required Texts/Readings

Textbook (required)

Semiconductor Devices: Physics and Technology 3rd ed., by S.M.Sze and M.K.Lee, John Wiley, 2012, ISBN 978-0-470-53794-7
EE221 covers most contents of chapters 1-7.

Other Readings (not required)

1. Solid State Electronic Devices, 6th ed., Ben G. Streetman, S.K. Banerjee, Prentice Hall, 2000
2. Physics and Technology of Semiconductor Devices, A.S. Grove, John Wiley, 1967.
3. Semiconductor Devices, S.M. Sze, John Wiley, 1985.
4. Device Electronics for Integrated Circuits, RS. Muller and T.I. Kamins, John Wiley, 1977.
5. VLSI Fabrication Principles, Sorab K. Ghandi, John Wiley, 1983.
6. VLSI Technology, S.M. Sze, McGraw- Hill, 1985.
7. Microelectronic Processing- An Introduction to Manufacturing Integrated Circuits, W. Scott Ruska, McGraw- Hill, 1987.
8. Electronic Materials Science for Integrated Circuits in Si and GaAs, Shyam P. Murarka and Martin C. Peckerer, Academic Press, 1989.
9. Electronic materials Science and Technology, James W. Mayer and S.S. Lau, Macmillan, 1990.)

Classroom Protocol

Students are expected to participate actively in class. Students should turn their cell phones off or put them on vibrate mode while in class. They will not answer their phones in class.

Assignments and Grading Policy

a. Homework

Homework is assigned and is posted online during the semester (usually one per chapter). Homework will be collected but not graded. The solutions will be posted in Canvas.

b. Exams

There are two mid-term examination and one final examination.

c. Class Participation:

Class participation is required, and student attendance will be checked. Dropping and Adding Students are responsible for understanding the policies and procedures about add/drops, academic renewal, etc. Information on add/drops are available at http://info.sjsu.edu/web-dbgen/narr/soc-fall/rec-298.html. Information about late drop is available at http://www.sjsu.edu/sac/advising/latedrops/policy/ **.** Students should be aware of the current deadlines and penalties for adding and dropping classes.

Grading Policy

Homework	5%
Mid-exam (2)	25% each
Quiz and Class Participation	10%
Final Exam	35%
Total	**100%**

Final Grade Percentage Breakdown

94% and above	A
93% - 90%	A-
89% - 80%	B+
79% - 70%	B
69% - 65%	B-
64% - 60%	C+
59% - 55%	C
54% - 50%	C-
49% - 45%	D+
44% - 40%	D
below 40%	F

University Policies

Academic integrity

Students should know that the University's Academic Integrity Policy is availabe at http://www.sa.sjsu.edu/download/judicial_affairs/Academic_Integrity_Policy_S07-2.pdf. Your own commitment to learning, as evidenced by your enrollment at San Jose State University and the University's integrity policy, require you to be honest in all your academic course work. Faculty members are required to report all infractions to the office of Student Conduct and Ethical Development. The website for Student Conduct and Ethical Development is available at http://www.sa.sjsu.edu/judicial_affairs/index.html.

Instances of academic dishonesty will not be tolerated. Cheating on exams or plagiarism (presenting the work of another as your own, or the use of another

person's ideas without giving proper credit) will result in a failing grade and sanctions by the University. For this class, all assignments are to be completed by the individual student unless otherwise specified. If you would like to include in your assignment any material you have submitted, or plan to submit for another class, please note that SJSU's Academic Policy F06-1 requires approval of instructors.

Campus Policy in Compliance with the American Disabilities Act

If you need course adaptations or accommodations because of a disability, or if you need to make special arrangements in case the building must be evacuated, please make an appointment with me as soon as possible, or see me during office hours. Presidential Directive 97-03 requires that students with disabilities requesting accommodations must register with the DRC (Disability Resource Center) to establish a record of their disability.

EE221, Section-1, Fall2017, Course Schedule

Week	Date	Topic	Reading
1	8/24	Class logistics and introduction to the course	Chapter1, 1.1-1.2
2	8/29 & 8/31	Energy bands and carrier concentration	Chapter 1: 1.3-1.6
3	9/5 & 9/7	Carrier transport, drift and diffusion	Chapter 2: 2: 21.-2.4
4	9/12 & 9/14	Carrier transport	Chapter 2: 2.5-2.8
5	9/19 & 9/21	p-n Junctions fabrication; equilibrium conditions	Chapter 3: 3.1-3.3
6	9/26 & 9/28	p-n junction operation, Heterojunction	Chapter 3: 3.4-3.7
7	10/3 & 10/5	**Review for exam, 1st exam 10/5/2017**	
8	10/10 & 10/12	Exam results discussion, Bipolar Transistor Fundamentals	Chapter 4: 4.1
9	10/17 &10/19	Frequency response and switching of BJT, Hetero-junction BJT	Chapter 4: 4.2 Chapter 4: 4.3-4.5
10	10/24 &10/26	The MOS Capacitor	Chapter5: 5.1
11	10/31 &11/2	SiO2/Si MOS capacitor	Chapter 5: 5.2-5.3
12	11/7 &11/9	**Review for exam, 2nd exam 11/9/2017**	
13	11/14 &11/16	Exam results discussion MOSFET fundamentals cont.	Chapter 5: 5.5
14	11/21	MOS scaling , CMOS, M-S contacts	Chapter 6: 6.1-6.5
14	11/23	**Thanksgiving Recess**	
15	11/28 & 11/30	M-S Contacts, MESFET	Chapter 7:7.1
16	12/5 &12/7	MESFET and MODFET **Review for final**	Chapter7: 7.2-7.3
17	**Final Examination: Thursday, December 14, 2:45 - 5:00pm**		

San Jose State University
Electrical Engineering Department

EE Department Honor Code

The Electrical Engineering Department will enforce the following Honor Code that must be read and accepted by all students.

"I have read the Honor Code and agree with its provisions. My continued enrollment in this course constitutes full acceptance of this code. I will NOT:

- *Take an exam in place of someone else, or have someone take an exam in my place*
- *Give information or receive information from another person during an exam*
- *Use more reference material during an exam than is allowed by the instructor*
- *Obtain a copy of an exam prior to the time it is given*
- *Alter an exam after it has been graded and then return it to the instructor for re-grading*
- *Leave the exam room without returning the exam to the instructor."*

Measures Dealing with Occurrences of Cheating

- *Department policy mandates that the student or students involved in cheating will receive an "F" on that evaluation instrument (paper, exam, project, homework, etc.) and will be reported to the Department and the University.*
- *A student's second offense in any course will result in a Department recommendation of suspension from the University.*