San José State University  
College of Engineering, Department of Electrical Engineering  
EE221-01, Principle of Semiconductor Devices I, Fall2019  

Course and Contact Information  
Instructor: Bhaskar L Mantha  
Office Location: Engineering Building/ENG 261  
Telephone: 925-413-8365  
Email: bhaskar.mantha@sjsu.edu  
Office Hours: Tu 4:30pm-05:30pm  
Class Days/Time: Tu Th 3:00pm-4:15pm  
Classroom: Engineering Building 343  
Prerequisites: EE128 or consent of instructor  

Faculty Web Page and MYSJSU Messaging  
Course materials such as syllabus, handouts, notes, assignment instructions, etc. can be found on my faculty web page at http://www.sjsu.edu/people/firstname.lastname and/or on Canvas Learning Management System course login website at http://sjsu.instructure.com. You are responsible for regularly checking with the messaging system through MySJSU on Spartan App Portal http://one.sjsu.edu (or other communication system as indicated by the instructor) to learn of any updates.  

Course Description  
This course is a prerequisite for all electronics area courses and reviews semiconductor device physics and technology. The students are expected to have some background in atomic physics and solid state physics for this course. The course is divided into four parts- semiconductor fundamentals, p-n junctions, bipolar junction transistors (BJT), and field effect transistors (FET). Semiconductor devices in equilibrium and non-equilibrium conditions will be discussed.  

Course Learning Outcomes (CLO)  

Upon successful completion of this course, students will be able to:  

LO1 Describe fundamental concepts of solid-state physics applied to the semiconductor devices of Silicon and compound semiconductor materials.  
LO2 Explain general electrical behavior of semiconductor Si and GaAs, construct appropriate physical models.  
LO3 Illustrate structural details and current-voltage characteristics of p-n junction diode, BJT, MOSFET, Metal/semiconductor diode, and MESFET.  
LO4 Apply the fundamental understandings of semiconductor devices with knowledge on the limitations of physical models.
Required Texts/Readings

EE221 covers most contents of chapters 0-7.

Other Readings (not required)


Other technology requirements / equipment / material

A scientific calculator is required for homework and exam.

Course Requirements and Assignments

Assignments

There is a homework assignment about every week or once in two weeks depending on the length of the chapter. The assignments will be announced in class and be posted in Canvas. The deadline will be posted in the same time. Usually one week of time will be given to finish an assignment. Homework will be submitted online in Canvas. Homework solution will be posted in Canvas after due date. Late homework submissions will not be accepted. One lowest homework score will be dropped for every student.

There are two midterm exams and one final exam. Exams cover the assigned reading materials and class lecture notes. There will be no make-up exams (only in very special circumstances, both written excuse and official proof are required for extraordinary situations). Mid-term exam solutions will be discussed in class after the exam date.

Success in this course is based on the expectation that students will spend, for each unit of credit, a minimum of 45 hours over the length of the course (normally three hours per unit per week) for instruction, preparation/studying, or course related activities, including but not limited to internships, labs, and clinical practice. Other course structures will have equivalent workload expectations as described in the syllabus.

Quizzes

There will be quiz given in class time for the length of 20 minutes every week. Quizzes normally cover the prior lecture contents. There is no make-up quiz. For every student, the lowest quiz score will be dropped in final counting.
Final Examination

*Final exam is comprehensive, covering the semiconductor device portion starting from chapter 5 (Junctions) to chapter 7 (BJTs). Samples of middle term exams and final exam are posted in Canvas course file folder. Please check these materials as the class progresses.*

Grading Policy

<table>
<thead>
<tr>
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<th>Percentage</th>
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<tbody>
<tr>
<td>Homework</td>
<td>5%</td>
</tr>
<tr>
<td>Mid-examinations</td>
<td>25% each</td>
</tr>
<tr>
<td>Quiz and Class Participation</td>
<td>10%</td>
</tr>
<tr>
<td>Final Exam</td>
<td>35%</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td><strong>100%</strong></td>
</tr>
</tbody>
</table>

Final Grade Percentage Breakdown

- 94% and above: A
- 93% - 90%: A minus
- 89% - 80%: B plus
- 79% - 70%: B
- 69% - 65%: B minus
- 64% - 60%: C plus
- 59% - 55%: C
- 54% - 50%: C minus
- 49% - 45%: D plus
- 44% - 40%: D
- below 40%: F

Classroom Protocol

Students are expected to participate actively in class. Students will turn their cell phones off or put them on vibrate mode while in class. They will not answer their phones in class.

Dropping and Adding

Students are responsible for understanding the policies and procedures about add/drops, academic renewal, etc. Information on add/drops are available at [http://info.sjsu.edu/web-dbgen/narr/soc-fall/rec-298.html](http://info.sjsu.edu/web-dbgen/narr/soc-fall/rec-298.html). Information about late drop is available at [http://www.sjsu.edu/sac/advising/latedrops/policy/](http://www.sjsu.edu/sac/advising/latedrops/policy/). Students should be aware of the current deadlines and penalties for adding and dropping classes.

University Policies

Academic Integrity

Students should know that the University’s Academic Integrity Policy is available at [http://www.sjsu.edu senate/docs/S16-9.pdf](http://www.sjsu.edu senate/docs/S16-9.pdf).

Relevant information such as academic integrity, accommodations, dropping and adding, consent for recording of class etc. is available at the office of Graduate and Undergraduate Program’s Syllabus Information web page at [http://www.sjsu.edu/gup/syllabusinfo/](http://www.sjsu.edu/gup/syllabusinfo/). Make sure you visit this page, review and be familiar with these university policies and resources.
Your own commitment to learning, as evidenced by your enrollment at San Jose State University and the University’s integrity policy, require you to be honest in all your academic course work. Faculty members are required to report all infractions to the office of Student Conduct and Ethical Development. The website for Student Conduct and Ethical Development is available at http://www.sa.sjsu.edu/judicial_affairs/index.html.

Instances of academic dishonesty will not be tolerated. Cheating on exams or plagiarism (presenting the work of another as your own, or the use of another person’s ideas without giving proper credit) will result in a failing grade and sanctions by the University. For this class, all assignments are to be completed by the individual student unless otherwise specified. If you would like to include in your assignment any material you have submitted, or plan to submit for another class, please note that SJSU’s Academic Policy F06-1 requires approval of instructors.

**Campus Policy in Compliance with the American Disabilities Act**

If you need course adaptations or accommodations because of a disability, or if you need to make special arrangements in case the building must be evacuated, please make an appointment with me as soon as possible, or see me during office hours. Presidential Directive 97-03 requires that students with disabilities requesting accommodations must register with the DRC (Disability Resource Center) to establish a record of their disability.

**EE Department Honor Code**

The Electrical Engineering Department will enforce the following Honor Code that must be read and accepted by all students.

“I have read the Honor Code and agree with its provisions. My continued enrollment in this course constitutes full acceptance of this code. I will NOT:

- Take an exam in place of someone else, or have someone take an exam in my place
- Give information or receive information from another person during an exam
- Use more reference material during an exam than is allowed by the instructor
- Obtain a copy of an exam prior to the time it is given
- Alter an exam after it has been graded and then return it to the instructor for re-grading
- Leave the exam room without returning the exam to the instructor.”

**Measures Dealing with Occurrences of Cheating**

- Department policy mandates that the student or students involved in cheating will receive an “F” on that evaluation instrument (paper, exam, project, homework, etc.) and will be reported to the Department and the University.
- A student’s second offense in any course will result in a Department recommendation of suspension from the University.
# EE221-01 / Principle of Semiconductor Device I, F2019

## Course Schedule: Schedule is tentative and subject to change

<table>
<thead>
<tr>
<th>Week</th>
<th>Date</th>
<th>Topics</th>
<th>Readings</th>
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<tbody>
<tr>
<td>1</td>
<td>8/22</td>
<td>Class logistics, Introduction to the course</td>
<td>Chapter 0</td>
</tr>
<tr>
<td>2</td>
<td>8/27, 8/29</td>
<td>Semiconductors, Crystal structures, Energy bands and carrier concentrations, Donors and Acceptors</td>
<td>Chapter 1: 1.1-1.6</td>
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<tr>
<td>3</td>
<td>9/3, 9/5</td>
<td>Carrier transport, drift and diffusion</td>
<td>Chapter 2: 2.1-2.4</td>
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<tr>
<td>4</td>
<td>9/10, 9/12</td>
<td>Carrier transport (other mechanisms)</td>
<td>Chapter 2: 2.5-2.8</td>
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<tr>
<td>5</td>
<td>9/17, 9/19</td>
<td>P-N Junctions, fabrication; equilibrium conditions</td>
<td>Chapter 3: 3.1-3.3</td>
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<tr>
<td>6</td>
<td>9/24, 9/26</td>
<td>P-N Junction operation, Hetero-junctions</td>
<td>Chapter 3: 3.4-3.7</td>
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<tr>
<td>7</td>
<td>10/1, 10/3</td>
<td>Review for 1st exam, <strong>1st Mid-Exam 10/3/2019</strong> Venue: Classroom</td>
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<tr>
<td>8</td>
<td>10/8, 10/10</td>
<td>Exam results discussion, Bipolar transistor fundamentals</td>
<td>Chapter 4: 4.1</td>
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<tr>
<td>9</td>
<td>10/15, 10/17</td>
<td>Frequency response and switching of BJT, Hetero-junction BJT</td>
<td>Chapter 4: 4.2</td>
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<td>Chapter 4: 4.3-4.5</td>
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<tr>
<td>10</td>
<td>10/22, 10/24</td>
<td>MOS FET: MOS Capacitor</td>
<td>Chapter 5: 5.1</td>
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<tr>
<td>11</td>
<td>10/29, 10/31</td>
<td>MOS Characteristics</td>
<td>Chapter 5: 5.2-5.3</td>
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<tr>
<td>12</td>
<td>11/5, 11/7</td>
<td>Review for 2nd exam, <strong>2nd Mid-Exam 11/7/2019</strong> Venue: Classroom</td>
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<td>13</td>
<td>11/12, 11/14</td>
<td>Exam results discussion, MOS Fundamental continue.</td>
<td>Chapter 5: 5.5</td>
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<tr>
<td>14</td>
<td>11/19, 11/21</td>
<td>MOS scaling, CMOS, M/S contacts</td>
<td>Chapter 6: 6.1-6.5</td>
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<tr>
<td>15</td>
<td>11/27, 11/28</td>
<td>M/S contacts, MESFET</td>
<td>Thanksgiving</td>
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<td></td>
<td>Chapter 7: 7.7.1</td>
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<tr>
<td>16</td>
<td>12/3, 12/5</td>
<td>MESFET and MODFET</td>
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<td>Chapter 7: 7.2-7.3</td>
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<tr>
<td>Final Exam</td>
<td>12/11/2019</td>
<td><strong>Wednesday, 12/11/2018, 2:45-5:00pm</strong> Venue: Classroom</td>
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