San José State University
Department of Electrical Engineering
EE 178: Digital Design with FPGAs, Section 1, Fall 2018

Course and Contact Information

Instructor:	Tan Van Nguyen
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Office Hours:	MW 17:45 – 19:30
Class Days/Time:	MW 16:30 – 17:45
Classroom:	Engineering Building 403
Prerequisites:	EE118 (with grade C or better)

Faculty Web Page and Messaging

Copies of the course materials such as the syllabus and assignments are found on the course web page at http://www.eric.crabill.org. You are responsible for regularly checking the course web page to learn of any updates. The instructor phone is provided for urgent or private matters only.

Course Description

This course will expose you to digital design with programmable logic devices using VerilogHDL. Additionally, you will learn about FPGA devices, synthesis and simulation, and additional topics applicable to synchronous systems.

Course Goals and Student Learning Objectives

The course goal is to provide a background, at an intermediate level, of a digital circuit design flow including capture in Verilog-HDL, synthesis, implementation, and hardware validation. Students will gain experience in application of the design flow using a state-of-the-art CAD tool and FPGA devices. ABET compliant learning objectives include, but are not limited to:

1. The ability to understand major selection criteria for implementation technologies and identify compelling advantages of FPGA devices.

2. The ability to understand and apply a hardware description language to capture design behavior and use that same hardware description language to exercise the captured design to evaluate its behavior.

3. The ability to use CAD software, tools, and instruments as part of a design flow to render digital circuits which meet their functional and performance specifications.

4. The ability to work in a group. Related, the ability to collaborate to prepare and present technical documentation of results.

Required Texts and Materials

Textbook

There is no required textbook for this course. The instructor will provide an URL to required supplemental reading material. The instructor will also provide electronic copies of the lecture and lab materials on the course web page.

Materials

- Digilent Basys3 board (Xilinx Artix 7 FPGA) from http://www.digilentinc.com
- Laptop or desktop PC with Microsoft Windows 10 (64-bit) and a USB port
- Xilinx Vivado 2016.2 Webpack Edition from http://www.xilinx.com

Other References

Your textbook from EE118 (or equivalent) serves as a fundamental reference.

Course Requirements and Assignments

All students have the right, within a reasonable time, to know their academic scores, to review their graded work, and to be provided with explanations for the determination of their course grades. Students may request a score summary by contacting the instructor.

To support ABET accreditation and deter violations of academic integrity and the honor code, the instructor keeps a copy of all submitted evaluation instruments of all students.
Late work is not accepted and receives zero credit. Please refer to the course schedule for lab, exam, and final presentation dates and times.

Final Examination or Evaluation

University policy requires an appropriate final examination or evaluation at the scheduled time in every course. In this course, the final evaluation consists of the final lab project and associated presentation, a team-based activity.

Grading Information

Lab Exercises:	Four, at 8% each: 32%
Lab Exercise Quizzes:	Four, at 3% each: 12%
Lab Projects:	Four, at 8% each: 32%
Concept Exams:	Two, at 8% each: 16%
Final Presentation:	One, at 8%: 8%

Grading Policy

A+	≥ 97	A	$\geq 93, < 97$	A-	$\geq 90, < 93$
B+	$\geq 87, < 90$	B	$\geq 83, < 87$	B-	$\geq 80, < 83$
C+	$\geq 77, < 80$	C	$\geq 73, < 77$	C-	$\geq 70, < 73$
D+	$\geq 67, < 70$	D	$\geq 63, < 67$	D-	$\geq 60, < 63$
F	< 60				

Classroom Protocol

Use common sense during lectures and office hours. Show respect for all members of the class. If you are not sure if something is allowed, ask.

Arrive on time, no food in class or lab, turn off cell phone, NO private discussion in class.

Honor Code

The Electrical Engineering Department will enforce the following honor code that must be read and accepted by all students:

I have read the honor code and agree with its provisions. My continued enrollment in this course constitutes full acceptance of this code. I will NOT:

- *Take an exam in place of someone, or have someone take an exam in my place*
- *Give information or receive information from another person during an exam*
- *Use more reference material during an exam than is allowed by the instructor*
- *Obtain a copy of an exam prior to the time it is given*
- *Alter an exam after it has been graded and then return it for re-grading* *Leave the exam room without returning the exam to the instructor* Measures Dealing with Occurrences of Cheating:
- Department policy mandates that the student or students involved in cheating will receive an "F" on that evaluation instrument (paper, exam, project, homework, etc.) and will be reported to the Department and the University
- A student's second offense will result in a Department recommendation of suspension

Professional Attitude

In addition to the honor code, students understand that a professional attitude is necessary to maintain a comfortable academic environment. For example:

- Do not skip the lecture and then later ask the instructor to summarize the lecture
- Come to the lectures on time and remain for the entire duration of the session
- To minimize possible tension during exams, follow the exam rules closely

University Policies (Required)

Per University Policy S16-9, university-wide policy information relevant to all courses, such as academic integrity, accommodations, etc. will be available on Office of Graduate and Undergraduate Programs' Syllabus Information web page at http://www.sjsu.edu/gup/syllabusinfo/" Make sure to review these policies and resources.

EE178: Digital Design with FPGAs, Fall 2018 Course Schedule

List the agenda for the semester including when and where the final exam will be held. Indicate the schedule is subject to change with fair notice and how the notice will be made available.

Course Schedule

Week	Date	Topics, Readings, Assignments, Deadlines
1	08/22	Administrative, Lab 1 Exercise assigned
2	08/27	UTH p.20 – p.27
2	08/29	Lab 1 Exercise due, Lab 1 Quiz, Lab 2 Project assigned
3	**09/03**	**No Class – Labor Day**
3	09/05	UTH p.75 – p.91
4	09/10	
4	09/12	UTH p.187 – p.193
5	09/17	Lab 2 Project due, Lab 3 Exercise assigned
5	09/19	UTH p.219 – p.229
6	09/24	Lab 3 Exercise due, Lab 3 Quiz, Concept Exam 1 prep
6	09/26	Concept Exam 1 [In Class]
7	10/01	Lab 4 Project assigned
7	10/03	UTH p.169 – p.181
8	10/08	
8	10/10	UTH p.182 – p.186
9	10/15	Lab 4 Project due, Lab 5 Exercise assigned
9	10/17	UTH p.93 – p.103
10	10/22	Lab 5 Exercise due, Lab 5 Quiz, Lab 6 Project assigned
10	10/24	
11	10/29	UTH p.103 – p.111
11	10/31	Lab 6 Project due, Concept Exam 2 prep
12	11/5	Concept Exam 2 [In Class]
12	11/7	UTH p.244 – p.251
13	**11/12**	**No Class - Veteran'**
13	11/14	Lab 7 Exercise assigned
14	11/19	UTH p.251 – p.256 04/26
14	**11/21**	**No Class – Thanksgiving**
15	11/26	Lab 7 Exercise due, Lab 7 Quiz, Lab 8 Project assigned
15	11/28	
16	12/04	Presentation prep
16	12/06	No Class – Conference Day
17	12/10	Lab 8 Project & Presentation, in classroom
17	12/13	Lab 8 Project & Presentation, in classroom 14:45 – 17:00