

San José State University
Department of Electrical Engineering
EE178, Digital Design with FPGAs, Spring 2018 (v1.0)

Instructor:	Eric Crabill
Office Location:	Engineering Building 339
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Office Hours:	TR 20:45 – 21:00 (see classroom protocol)
Class Days/Time:	TR 19:30 – 20:45
Classroom:	Engineering Building 339
Prerequisites:	EE118 (with grade C or better)

Course Web Page and Messaging

Copies of the course materials such as the syllabus and assignments are found on the course web page at <http://www.eric.crabill.org>. You are responsible for regularly checking the course web page to learn of any updates. The instructor phone is provided for urgent or private matters only.

Course Description

This course will expose you to digital design with programmable logic devices using Verilog-HDL. Additionally, you will learn about FPGA devices, synthesis and simulation, and additional topics applicable to synchronous systems.

Course Goals and Student Learning Objectives

The course goal is to provide a background, at an intermediate level, of a digital circuit design flow including capture in Verilog-HDL, synthesis, implementation, and hardware validation. Students will gain experience in application of the design flow using a state-of-the-art CAD tool and FPGA devices. ABET compliant learning objectives include, but are not limited to:

1. The ability to understand major selection criteria for implementation technologies and identify compelling advantages of FPGA devices.
2. The ability to understand and apply a hardware description language to capture design behavior and use that same hardware description language to exercise the captured design to evaluate its behavior.
3. The ability to use CAD software, tools, and instruments as part of a design flow to render digital circuits which meet their functional and performance specifications.
4. The ability to work in a group. Related, the ability to collaborate to prepare and present technical documentation of results.

Course Policies

Use common sense during lectures and office hours. Show respect for all members of the class. If you are not sure if something is allowed, ask.

Posted office hours are the 15 minutes following the official meeting time. It is the instructor's policy to answer all questions brought by students, so office hours may run substantially longer. To prevent abuse of the "no question left unanswered" policy, you must arrive in the officially scheduled 15 minutes and add your name to the waiting list. Please advise the instructor promptly if you have a schedule or transportation constraint which may require re-prioritization of your name on the waiting list.

Department Policies

Honor Code

The Electrical Engineering Department will enforce the following honor code that must be read and accepted by all students:

I have read the honor code and agree with its provisions. My continued enrollment in this course constitutes full acceptance of this code. I will NOT:

- *Take an exam in place of someone, or have someone take an exam in my place*
- *Give information or receive information from another person during an exam*
- *Use more reference material during an exam than is allowed by the instructor*
- *Obtain a copy of an exam prior to the time it is given*
- *Alter an exam after it has been graded and then return it for re-grading*
- *Leave the exam room without returning the exam to the instructor*

Measures Dealing with Occurrences of Cheating:

- Department policy mandates that the student or students involved in cheating will receive an "F" on that evaluation instrument (paper, exam, project, homework, etc.) and will be reported to the Department and the University
- A student's second offense will result in a Department recommendation of suspension

Professional Attitude

In addition to the honor code, students understand that a professional attitude is necessary to maintain a comfortable academic environment. For example:

- Do not skip the lecture and then later ask the instructor to summarize the lecture
- Come to the lectures on time and remain for the entire duration of the session
- To minimize possible tension during exams, follow the exam rules closely

University Policies

Per University Policy S16-9, university-wide policy information relevant to all courses, such as academic integrity, accommodations, etc. is available from the Office of Graduate and Undergraduate Programs at <http://www.sjsu.edu/gup/syllabusinfo>.

Required Texts and Materials

Required Textbook

There is no required textbook for this course. The instructor will provide an URL to required supplemental reading material. The instructor will also provide electronic copies of the lecture and lab materials on the course web page.

Required Materials

- Digilent Basys3 board (Xilinx Artix 7 FPGA) from <http://www.digilentinc.com>
- Laptop or desktop PC with Microsoft Windows 10 (64-bit) and a USB port
- Xilinx Vivado 2016.2 Webpack Edition from <http://www.xilinx.com>

Other References

Your textbook from EE118 (or equivalent) serves as a fundamental reference.

Assignments and Grading Policy

All students have the right, within a reasonable time, to know their academic scores, to review their graded work, and to be provided with explanations for the determination of their course grades. Students may request a score summary by contacting the instructor.

Evaluation Instruments

Lab Exercises:	Four, at 8% each: 32%
Lab Exercise Quizzes:	Four, at 3% each: 12%
Lab Projects:	Four, at 8% each: 32%
Concept Exams:	Two, at 8% each: 16%
Final Presentation:	One, at 8%: 8%

Grading Policy

A+	≥ 97	A	$\geq 93, < 97$	A-	$\geq 90, < 93$
B+	$\geq 87, < 90$	B	$\geq 83, < 87$	B-	$\geq 80, < 83$
C+	$\geq 77, < 80$	C	$\geq 73, < 77$	C-	$\geq 70, < 73$
D+	$\geq 67, < 70$	D	$\geq 63, < 67$	D-	$\geq 60, < 63$
F	< 60				

To support ABET accreditation, and deter violations of academic integrity and the honor code, the instructor keeps a copy of all submitted evaluation instruments of all students.

Late work is not accepted and receives zero credit. Please refer to the course schedule for lab, exam, and final presentation dates and times.

Final Evaluation

University policy requires an appropriate final examination or evaluation at the scheduled time in every course. In this course, the final evaluation consists of the final lab project and associated presentation, a team-based activity.

EE178, Digital Design with FPGAs, Spring 2018, Course Schedule

The schedule is subject to change with fair notice. If a change is necessary, it will be communicated via email through MySJSU.

Wk	Date	Assignments, Deadlines	Readings
1	01/23 01/25	No Class – Conference Day Administrative, Lab 1 Exercise assigned	NONE
2	01/30 02/01	Lab 1 Exercise due, Lab 1 Quiz, Lab 2 Project assigned	UTH p.20 – p.27
3	02/06 02/08		UTH p.75 – p.91
4	02/13 02/15	Lab 2 Project due, Lab 3 Exercise assigned	UTH p.187 – p.193
5	02/20 02/22	Lab 3 Exercise due, Lab 3 Quiz, Concept Exam 1 prep	UTH p.219 – p.229
6	02/27 03/01	Concept Exam 1 [In Class] Lab 4 Project assigned	NONE
7	03/06 03/08		UTH p.169 – p.181
8	03/13 03/15	Lab 4 Project due, Lab 5 Exercise assigned	UTH p.182 – p.186
9	03/20 03/22	Lab 5 Exercise due, Lab 5 Quiz, Lab 6 Project assigned	UTH p.93 – p.103
10	03/27 03/29	No Class – Spring Break No Class – Spring Break	NONE
11	04/03 04/05		UTH p.103 – p.111
12	04/10 04/12	Lab 6 Project due, Concept Exam 2 prep Concept Exam 2 [In Class]	NONE
13	04/17 04/19	Lab 7 Exercise assigned	UTH p.244 – p.251
14	04/24 04/26	Lab 7 Exercise due, Lab 7 Quiz, Lab 8 Project assigned Lab 8 Proposal due	UTH p.251 – p.256
15	05/01 05/03		NONE
16	05/08 05/10	Presentation prep	NONE
17	05/15 05/17	No Class – Conference Day Lab 8 Project & Presentation, in classroom, 19:45 to 22:00	NONE