San José State University Department of Electrical Engineering
EE178 Section 1, Digital Design with FPGAs, Spring 2021 (v1.0)

Course and Contact Information

Instructor: Christopher Pham
Office Location: Office Hour Meeting Information: See Canvas for details
Telephone: (408) 924-3950
Email: Christopher.h.pham01@sjsu.edu
Office Days/Time: TR after class hours 8:45pm-9:30pm
Class Days/Time: TR 19:30 – 20:45
Classroom: Zoom Meeting Information: See Canvas for details
Prerequisites: EE118 with grade C minus or better

Course Description

This course will expose students to digital design with programmable logic devices using Verilog-HDL. Additionally, students will learn about field programmable devices, synthesis and simulation, and additional topics applicable to synchronous systems.

Course Format

Technology Intensive, Hybrid, and Online Courses
The course is instructed in a hybrid format. Students are required to have access to an electronic device to follow along in class, and for homework. The electronic device must be able to run complex engineering applications such as Xilinx Vivado and Vitis Design Suites and analytics tools used in this class.

This course is a technology intensive course which requires access to specified hardware and software for completion of assignments. Additionally, mobile internet connectivity is required. Continued enrollment in this course signifies student understanding and acceptance of the required texts and materials.

Course Goal and Learning Outcomes

The course goal is to provide a background, at an intermediate level, of a digital circuit design flow including capture in Verilog-HDL, synthesis, implementation, and hardware validation. Students will gain experience in application of a state-of-the-art CAD tool and field programmable devices to implement functionally correct designs meeting performance requirements. ABET compliant course learning outcomes include:

- The ability to understand and apply a hardware description language to capture design behavior and use that same hardware description language to exercise the captured design to evaluate its behavior. [ABET Student Outcome 1]
- The ability to use CAD software, tools, and instruments as part of a design flow to render digital circuits which meet their functional and performance specifications. [ABET Student Outcome 2]
- The ability to recognize design aspects that can affect reliability and make informed judgments given potential impacts to environmental, safety, economic, and legal contexts. [ABET Student Outcome 4]
• The ability to work in a group. Related, the ability to collaborate to prepare and present technical
documentation of results at appropriate levels of detail for the target audiences. [ABET Student
Outcomes 3 and 5]
• The ability to understand major selection criteria for implementation technologies and identify
compelling advantages of field programmable devices. [ABET Student Outcome 7]

Required Texts and Materials

Required Textbook
There is no required textbook. The instructor will provide all required reading material through Canvas.

Required Materials
• Real Digital Blackboard from https://www.realdigital.org (~$175, delivered, academic pricing)
• Xilinx+Vitis Vivado 2020.2 or later Webpack Edition from https://www.xilinx.com
• Laptop PC with Microsoft Windows 10 (64-bit) and a USB port, Intel Core i7 or higher recommended

Other References
A textbook from EE118 (or equivalent) serves as a fundamental reference for digital logic design principles.
A Verilog-HDL textbook. There will be two public-domain textbooks for download.
A C-language textbook.

Requirements
Success in this course is based on the expectation that students will spend, for this 3-unit course, a minimum of
135 hours over the length of the course (normally 9 hours per week) for instruction, preparation and studying,
and course related activities, including but not limited to labs and projects. Please refer to the course schedule
for dates and times of labs, quizzes, exams, and presentations. University policy requires an appropriate final
examination or evaluation at the scheduled time in every course. In this course, the final evaluation consists of
the final lab project and an associated presentation, a team-based activity.

Assignments
Labs Seven, at 10% each: 70% total

Examination and Evaluation
Final Project (a.k.a. Lab 8): One: 20%
Final Exam One: 10%

Missed or late work and no-show policy
• Missed work is equivalent to zero credit. Late submissions are not accepted and will count as zeroes.
• Final Project must be submitted by the assigned due date and time before the final exam date and time.
  Missed final exam or final project participation will earn zero credit. No late submission is allowed.

Extra Credit
• Extra credit opportunity may be available throughout the semester.

Determination of Grades

<table>
<thead>
<tr>
<th>Grade</th>
<th>Percentage</th>
<th>Percentage</th>
</tr>
</thead>
<tbody>
<tr>
<td>A plus  &gt; 100</td>
<td>A = 96-100</td>
<td>A minus = 90-95.9999</td>
</tr>
<tr>
<td>B plus = 87-89.9999</td>
<td>B = 84-86.9999</td>
<td>B minus = 80-83.9999</td>
</tr>
<tr>
<td>C plus = 77-79.9999</td>
<td>C = 74-76.9999</td>
<td>C minus = 70-73.9999</td>
</tr>
<tr>
<td>D plus = 68-69.9999</td>
<td>D = 64-67.9999</td>
<td>D minus = 60-63.9999</td>
</tr>
<tr>
<td>F = 0-59.9999</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Digital Design with FPGAs, EE178 Section 1, Spring, 2021
Classroom Protocol
As a graduating elective course, this class resembles the enterprise level working environment. Ethics and professionalism in the workplace will be enforced.

University Policies
Per University Policy S16-9 (http://www.sjsu.edu/senate/docs/S16-9.pdf), relevant information to all courses, such as academic integrity, accommodations, dropping and adding, consent for recording of class, etc. is available on Office of Graduate and Undergraduate Programs’ Syllabus Information web page at http://www.sjsu.edu/gup/syllabusinfo/”. Make sure to visit this page, review and be familiar with these university policies and resources.

Related Policies
To support ABET accreditation, and deter violations of academic integrity and the honor code, the instructor keeps a copy of all submitted evaluation instruments of all students for at least two years. Late work without advanced agreement with the instructor is not accepted and receives zero credit. No extra credit assignments are given. All students have the right, within a reasonable time, to know their academic scores, to review their graded work, and to be provided with explanations for the determination of their course grades. Students may request a score summary by contacting the instructor. The incomplete “I” grade is reserved for unforeseeable, serious, and compelling reasons only.

Course Policies
Use common sense during lectures and office hours. Show respect for all members of the class. If unsure something is allowed, ask. Recording lectures in any format is prohibited. Posted office hours are the 15 minutes following the official meeting time. It is the instructor’s policy to answer all questions brought by students, so office hours may run substantially longer. To prevent abuse of the “no question left unanswered” policy, students must arrive in the officially scheduled 15 minutes and add their name to the waiting list. Please advise the instructor promptly of schedule or constraints which may require re-prioritization of the waiting list.

Professional Attitude
In addition to the honor code, students understand that a professional attitude is necessary to maintain a comfortable academic environment. As examples:

- Do not skip the lecture. If you have an emergency and cannot attend the lecture, review the Zoom recording of the lecture.
- Come to the lectures on time and remain for the entire duration of the session.
- To minimize possible tension during exams, follow the exam rules closely.

General Expectations, Rights and Responsibilities of the Student
As members of the academic community, students accept both the rights and responsibilities incumbent upon all members of the institution. Students are encouraged to familiarize themselves with SJSU’s policies and practices pertaining to the procedures to follow if and when questions or concerns about a class arises. See University Policy S90–5 at http://www.sjsu.edu/senate/docs/S90-5.pdf. More detailed information on a variety of related topics is available in the SJSU catalog, at http://info.sjsu.edu/home/catalog.html. In general, it is recommended that students begin by seeking clarification or discussing concerns with their instructor. If such conversation is not possible, or if it does not serve to address the issue, it is recommended that the student contact the Department Chair as a next step.
Dropping and Adding

Students are responsible for understanding the policies and procedures about add/drop, grade forgiveness, etc. Refer to the current semester’s Catalog Policies section at [http://info.sjsu.edu/static/catalog/policies.html](http://info.sjsu.edu/static/catalog/policies.html). Add/drop deadlines can be found on the current academic calendar web page located at [http://www.sjsu.edu/calendars/](http://www.sjsu.edu/calendars/). The Late Drop Policy is available at [http://www.sjsu.edu/aars/policies/latedrops/policy/](http://www.sjsu.edu/aars/policies/latedrops/policy/). Students should be aware of the current deadlines and penalties for dropping classes. Information about the latest changes and news is available at the Advising Hub at [http://www.sjsu.edu/advising/](http://www.sjsu.edu/advising/).

Consent for Recording of Class and Public Sharing of Instructor Material

[University Policy S12-7](http://www.sjsu.edu/senate/docs/S12-7.pdf), requires students to obtain instructor’s permission to record the course and the following items to be included in the syllabus:

− “Common courtesy and professional behavior dictate that you notify someone when you are recording him/her. You must obtain the instructor’s permission to make audio or video recordings in this class. Such permission allows the recordings to be used for your private, study purposes only. The recordings are the intellectual property of the instructor; you have not been given any rights to reproduce or distribute the material.”
  • It is suggested that the greensheet include the instructor’s process for granting permission, whether in writing or orally and whether for the whole semester or on a class by class basis.
  • In classes where active participation of students or guests may be on the recording, permission of those students or guests should be obtained as well.

− “Course material developed by the instructor is the intellectual property of the instructor and cannot be shared publicly without his/her approval. You may not publicly share or upload instructor generated material for this course such as exam questions, lecture notes, or homework solutions without instructor consent.”

Academic integrity

Your commitment as a student to learning is evidenced by your enrollment at San Jose State University. The University’s Academic Integrity policy, located at [http://www.sjsu.edu/senate/policies/pol_plagarism_acad_integrity/index.html](http://www.sjsu.edu/senate/policies/pol_plagarism_acad_integrity/index.html), requires you to be honest in all your academic course work. Faculty members are required to report all infractions to the office of Student Conduct and Ethical Development. The Student Conduct and Ethical Development website is available at [http://www.sjsu.edu/studentconduct/](http://www.sjsu.edu/studentconduct/)

Instances of academic dishonesty will not be tolerated. Cheating on exams or plagiarism (presenting the work of another as your own, or the use of another person’s ideas without giving proper credit) will result in a failing grade and sanctions by the University. For this class, all assignments are to be completed by the individual student unless otherwise specified. If you would like to include your assignment or any material you have submitted, or plan to submit for another class, please note that SJSU’s Academic Policy S07-2 requires approval of instructors.

Campus Policy in Compliance with the American Disabilities Act

If you need course adaptations or accommodations because of a disability, or if you need to make special arrangements in case the building must be evacuated, please make an appointment with me as soon as possible, or see me during office hours. Presidential Directive 97-03 at [http://www.sjsu.edu/president/docs/directives/PD_1997-03.pdf](http://www.sjsu.edu/president/docs/directives/PD_1997-03.pdf) requires that students with disabilities requesting accommodations must register with the Accessible Education Center (AEC) at [http://www.sjsu.edu/aec/](http://www.sjsu.edu/aec/) to establish a record of their disability.
EE Honor Code - Honesty and Respect for Others and Public Property

The Electrical Engineering Department will enforce the following Honor Code that must be read and accepted by all students.

“I have read the Honor Code and agree with its provisions. My continued enrollment in this course constitutes full acceptance of this code. I will NOT:

− Take an exam in place of someone else, or have someone take an exam in my place
− Give information or receive information from another person during an exam
− Copy project information from others
− Use more reference material during an exam than is allowed by the instructor
− Obtain a copy of an exam prior to the time it is given
− Alter an exam after it has been graded and then return it to the instructor for re-grading
− Leave the exam room without returning the exam to the instructor.”

Measures Dealing with Occurrences of Cheating

− Department policy mandates that the student or students involved in cheating will receive an “F” on that evaluation instrument (paper, exam, project, homework, etc.) and will be reported to the Department and the University.
− A student’s second offense in any course will result in a Department recommendation of suspension from the University.
# EE178, Digital Design with FPGAs, Spring 2020, Course Schedule

*The course schedule is subject to change with fair notice. If a change is necessary, it will be communicated via messaging through MySJSU Canvas and/or classroom announcements.*

## Tentative Course Schedule

<table>
<thead>
<tr>
<th>Week</th>
<th>Date</th>
<th>Assignments, Deadlines</th>
<th>Readings</th>
</tr>
</thead>
</table>
| 1    | Thursday 1/28/2021 | First day of instruction
Administrative, Lab 0 Assigned
Module 1 – Class Overview                         | NONE         |
| 2    | 2/2 and 2/4    | Lab 0 Exercise Due, Lab 1 Assigned
Module 2 - Review of Verilog HDL                      | UTH Chapter 1 |
| 3    | 2/9 and 2/11   | Lab 1 Due
Lab 2 Assigned – 7-segment Displays
Review of Verilog HDL – Coding Examples               | UTH Chapter 2 |
| 4    | 2/16 and 2/18  | Lab 2 Due, Lab 3 Assigned
Review of Verilog HDL – FSM Coding Examples           | UTH Chapter 3 |
| 5    | 2/23 and 2/25  | Lab 3 Due
Lab 4 Assigned – Digital Piano                       | UTH Chapter 4 |
| 6    | 3/2 and 3/4    | Module 3 – Static timing analysis                                                   | NONE         |
| 7    | 3/9 and 3/11   | Lab 4 Due
Lab 5 Assigned – FSM and IP Core                   | UTH Chapter 5 |
| 8    | 3/16 and 3/18  | Module 4 – Performance Improvement Techniques                                        | UTH Chapter 6 |
| 9    | 3/23 and 3/25  | Lab 5 Due
Lab 6 Assigned – Speech Synthesizing                 | UTH Chapter 7 |
| 10   | 3/30 and 4/1   | *Spring Recess from 3/29 to 4/2*                                                      | UTH Chapter 8 |
| 11   | 4/6 and 4/8    | Module 5 – Clock Management,
Synchronous/Asynchronous design techniques
Lab 6 Due                                              | NONE         |
| 12   | 4/13 and 4/15  | Module 6 – Hardware/Software Codesign
Lab 7 Assigned – Hardware/Software Codesign          | UTH Chapter 9 |
| 13   | 4/20 and 4/22  | Module 6 – Continued
Final Project Assigned                                 | NONE         |
| 14   | 4/27 and 4/29  | Lab 7 Due
Final Project Prep                                     | UTH Chapter 12 |
| 15   | 5/4 and 5/6    | Final Project Prep                                                                    | UTH Chapter 11|
| 16   | 5/11 and 5/13  | Final Project (Lab 8) due on 5/11/2021
Final Project Presentation                           | UTH Chapter 10 |
| 17   | 5/18 and 5/20  | No Class                                                                             |              |
| 18   | Tuesday, 5/25/2021 | Final Exam                                                                         | NONE         |
**FINAL EXAM SCHEDULE – Spring 2021**

https://www.sjsu.edu/classes/final-exam-schedule/spring-2021.php

**Night Classes**

Late afternoon and night classes meeting more than once per week should schedule their final exam on the earliest possible date. Example: final exam for ENGL 1A which meets on MWF from 1830-1945 should be scheduled on Wednesday, May 19 from 1945-2200 (not Monday, May 24).

<table>
<thead>
<tr>
<th>Regular Class Start Time</th>
<th>Final Examination Day</th>
<th>Final Examination Time</th>
</tr>
</thead>
<tbody>
<tr>
<td>Monday Night (1830 or later)</td>
<td>Monday, May 24</td>
<td>1945-2200</td>
</tr>
<tr>
<td>Tuesday Night (1830 or later)</td>
<td>Tuesday, May 25</td>
<td>1945-2200</td>
</tr>
<tr>
<td>Wednesday Night (1830 or later)</td>
<td>Wednesday, May 19</td>
<td>1945-2200</td>
</tr>
<tr>
<td>Thursday Night (1830 or later)</td>
<td>Thursday, May 20</td>
<td>1945-2200</td>
</tr>
<tr>
<td>Friday Night (1830 or later)</td>
<td>Friday, May 21</td>
<td>1945-2200</td>
</tr>
</tbody>
</table>

https://www.sjsu.edu/classes/calendar/2020-2021.php

<table>
<thead>
<tr>
<th>Event</th>
<th>Start Date</th>
<th>End Date</th>
</tr>
</thead>
<tbody>
<tr>
<td>Advance Registration Ends</td>
<td>August 16, 2020</td>
<td>January 24, 2021</td>
</tr>
<tr>
<td>No Registration Activity on MySJSU</td>
<td>August 17 - 18, 2021</td>
<td>January 25 - 26, 2021</td>
</tr>
<tr>
<td>First Day of Instruction</td>
<td>August 19, 2020</td>
<td>January 27, 2021</td>
</tr>
<tr>
<td>Late Registration Period Begins on MySJSU</td>
<td>- September 8, 2020</td>
<td>- February 15, 2021</td>
</tr>
<tr>
<td>Last Day to Drop Classes without a &quot;W&quot; grade</td>
<td>August 31, 2020</td>
<td>February 8, 2021</td>
</tr>
<tr>
<td>Last Day to Add Courses via MySJSU</td>
<td>September 8, 2020</td>
<td>February 15, 2021</td>
</tr>
<tr>
<td>Last Day to Submit Audit [pdf], Credit/No-Credit [pdf] Option Request</td>
<td>September 8, 2020</td>
<td>February 15, 2021</td>
</tr>
<tr>
<td>Last Day to Submit Instructor Drops</td>
<td>September 8, 2020</td>
<td>February 15, 2021</td>
</tr>
<tr>
<td>Last Day to Late Drop/Withdraw</td>
<td>November 13, 2020</td>
<td>April 22, 2021</td>
</tr>
<tr>
<td>Semester Withdrawal Deadline</td>
<td>November 13, 2020</td>
<td>April 22, 2021</td>
</tr>
</tbody>
</table>
2020-2021 Academic Year

**Academic Year** August 17, 2020 to May 28, 2021

**Fall Semester** August 19, 2020 to December 18, 2020

**Spring Semester** January 25, 2021 to May 28, 2021

<table>
<thead>
<tr>
<th>Event</th>
<th>Fall 2020</th>
<th>Spring 2021</th>
</tr>
</thead>
<tbody>
<tr>
<td>First Day of Instruction</td>
<td>August 19, 2020</td>
<td>January 27, 2021</td>
</tr>
<tr>
<td>Enrollment Census Date</td>
<td>September 16, 2020</td>
<td>February 23, 2021</td>
</tr>
<tr>
<td>Last Day of Instruction</td>
<td>December 7, 2020</td>
<td>May 17, 2021</td>
</tr>
</tbody>
</table>

**Holidays / No Classes**

<table>
<thead>
<tr>
<th>Event</th>
<th>Fall 2020</th>
<th>Spring 2021</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dr. Martin Luther King, Jr. Day</td>
<td>Campus Closed</td>
<td>January 18, 2021</td>
</tr>
<tr>
<td>Cesar Chavez Day</td>
<td>Campus Closed</td>
<td>March 31, 2021</td>
</tr>
<tr>
<td>Spring Recess</td>
<td>No Classes</td>
<td>March 29, 2021</td>
</tr>
<tr>
<td></td>
<td>- April 2, 2021</td>
<td></td>
</tr>
<tr>
<td>Spring 2021 Study/Conf. Day</td>
<td>No Classes or Exams</td>
<td>May 18, 2021</td>
</tr>
<tr>
<td>Memorial Day</td>
<td>Campus Closed</td>
<td>May 31, 2021</td>
</tr>
</tbody>
</table>