

**San José State University**  
**Electrical Engineering Department**  
**EE174: Analog Peripheral for Embedded Systems**  
**Section 1, Spring 2018**

**Course and Contact Information**

<b>Instructor:</b>	Tan Van Nguyen
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<b>Office Hours:</b>	MW 19:00-19:30 and after class or by appointment
<b>Class Code/Days/Time:</b>	22109, MW 19:30-20:45
<b>Classroom:</b>	ENG 401
<b>Prerequisites:</b>	EE110 and EE112 with C grade or better
<b>Lab Room:</b>	ENG 244 (If needed)

**Faculty Web Page**

Course materials such as syllabus, handouts, lecture notes, lab assignment instructions and homework can be found on my faculty web page at <http://www.sjsu.edu/people/tan.v.nguyen/courses>.

**Course Description**

Introduction to analog peripherals for embedded systems such as ADC/DAC, DC-DC Converters, Energy harvesting and solar cells, near field communication, RF-IDs, phase lock loops, clock generators, displays and touch screens. Industry based projects and applications are integral to the course.

**Learning Objectives**

1. Students will be able to design Op-Amp circuits and understand thoroughly Op-amp specifications and applications
2. Students will be able to explain the challenges of the Data conversion and associated performance metrics such as INL, DNL, ENOB, SNDR.
3. Students will be able to design DC to DC convertor and understand different architecture and associated performance metrics such as efficiency, loading.

4. Students will be able to evaluate different techniques and methods for energy harvesting in an embedded system.
5. Students will be able to develop a short range communication using standard protocols such as NFC and RFID
6. Students will be able to construct clock generator and understand the phase locking concepts and associated performance metrics such as jitter, eye-opening, skew, phase noise.
7. Students will be able to develop image sensing and displays system using an embedded system.

### **Course Goals**

This course introduces analog peripherals for embedded systems. In an embedded system on top of a general purpose microcontroller or DSP processor, there are other components to talk to the outside world. These components, peripherals, are such as Data converters, DC-DC Converters, Energy harvesting, solar cells, near field communication (NFC), RF-IDs, phase lock loops and clock generators, displays and touch screens. The course aims to establish an environment to expose students to other important block in embedded system architecture. This platform will be based on technical discussion, and lab experiences. The goal is students gain technical expertise to design and develop peripherals system in conjunction with an embedded system.

### **Required Texts/Readings**

#### **Textbook**

Instructor notes and handouts.

#### **Other Readings**

Different white papers, hardware and software tools by vendors.

### **Course Requirements and Assignments**

SJSU classes are designed such that in order to be successful, it is expected that students will spend a minimum of forty-five hours for each unit of credit (normally three hours per unit per week), including preparing for class, participating in course activities, completing assignments, and so on. More details about student workload can be found in [University Policy S12-3](http://www.sjsu.edu/senate/docs/S12-3.pdf) at <http://www.sjsu.edu/senate/docs/S12-3.pdf>.

Other course structures will have equivalent workload expectations as described in the syllabus.

### **Labs and Projects**

There are several labs and one project for this course. Project is mainly based on designing an embedded system application, using studied analog peripherals such as ADC, PLL, Display, NFC. Each group (maximum 3 students) must write a formal project report using a word processor (i.e. Microsoft Office) and submit the original write-up.

### **Quizzes and Homework**

There are two midterm examinations and several quizzes/homework for this course. There will be no make-up exam or quizzes and those absent will receive no credit. Students must write their answers clearly in an organized fashion. Further instructions will be provided during exams.

## Grading Policy

There will be no make-up exams/quizzes and those absent will receive no credit. Students must write their answers clearly in an organized fashion. Further instructions will be provided during exams. This course must be passed with a C or better as a CSU graduation requirement.

Exam 1	15%
Exam 2	15%
Homework/Quizzes	10%
Labs	20%
Design Project	15%
Final Exam	25%

### Grading Percentage Breakdown:

90% and above A  
 89% - 85% A-  
 84% - 82% B+  
 81% - 79% B  
 78% - 75% B-  
 74% - 72% C+  
 71% - 69% C  
 68% - 65% C-  
 64% - 62% D+  
 61% - 59% D  
 58% - 55% D  
 below 55% F

## Classroom Protocol

Arrive on time, no food in class or lab, turn off cell phone, NO private discussion in class.

## University Policies

### General Expectations, Rights and Responsibilities of the Student

As members of the academic community, students accept both the rights and responsibilities incumbent upon all members of the institution. Students are encouraged to familiarize themselves with SJSU's policies and practices pertaining to the procedures to follow if and when questions or concerns about a class arises. See [University Policy S90-5](#) at <http://www.sjsu.edu/senate/docs/S90-5.pdf>. More detailed information on a variety of related topics is available in the [SJSU catalog](#), at <http://info.sjsu.edu/web-dbgen/narr/catalog/rec-12234.12506.html>. In general, it is recommended that students begin by seeking clarification or discussing concerns with their instructor. If such conversation is not possible, or if it does not serve to address the issue, it is recommended that the student contact the Department Chair as a next step.

## Dropping and Adding

Students are responsible for understanding the policies and procedures about add/drop, grade forgiveness, etc. Refer to the current semester's [Catalog Policies](http://info.sjsu.edu/static/catalog/policies.html) section at <http://info.sjsu.edu/static/catalog/policies.html>. Add/drop deadlines can be found on the current academic year calendars document on the [Academic Calendars webpage](http://www.sjsu.edu/provost/services/academic_calendars/) at [http://www.sjsu.edu/provost/services/academic\\_calendars/](http://www.sjsu.edu/provost/services/academic_calendars/). The [Late Drop Policy](http://www.sjsu.edu/aars/policies/latedrops/policy/) is available at <http://www.sjsu.edu/aars/policies/latedrops/policy/>. Students should be aware of the current deadlines and penalties for dropping classes.

Information about the latest changes and news is available at the [Advising Hub](http://www.sjsu.edu/advising/) at <http://www.sjsu.edu/advising/>.

## Consent for Recording of Class and Public Sharing of Instructor Material

[University Policy S12-7](http://www.sjsu.edu/senate/docs/S12-7.pdf), <http://www.sjsu.edu/senate/docs/S12-7.pdf>, requires students to obtain instructor's permission to record the course and the following items to be included in the syllabus:

- “Common courtesy and professional behavior dictate that you notify someone when you are recording him/her. You must obtain the instructor's permission to make audio or video recordings in this class. Such permission allows the recordings to be used for your private, study purposes only. The recordings are the intellectual property of the instructor; you have not been given any rights to reproduce or distribute the material.”
  - It is suggested that the greensheet include the instructor's process for granting permission, whether in writing or orally and whether for the whole semester or on a class by class basis.
  - In classes where active participation of students or guests may be on the recording, permission of those students or guests should be obtained as well.
- “Course material developed by the instructor is the intellectual property of the instructor and cannot be shared publicly without his/her approval. You may not publicly share or upload instructor generated material for this course such as exam questions, lecture notes, or homework solutions without instructor consent.”

## Academic integrity

Your commitment, as a student, to learning is evidenced by your enrollment at San Jose State University. The [University Academic Integrity Policy S07-2](http://www.sjsu.edu/senate/docs/S07-2.pdf) at <http://www.sjsu.edu/senate/docs/S07-2.pdf> requires you to be honest in all your academic course work. Faculty members are required to report all infractions to the office of Student Conduct and Ethical Development. The [Student Conduct and Ethical Development website](http://www.sjsu.edu/studentconduct/) is available at <http://www.sjsu.edu/studentconduct/>.

## Campus Policy in Compliance with the American Disabilities Act

If you need course adaptations or accommodations because of a disability, or if you need to make special arrangements in case the building must be evacuated, please make an appointment with me as soon as possible, or see me during office hours. [Presidential Directive 97-03](http://www.sjsu.edu/president/docs/directives/PD_1997-03.pdf) at [http://www.sjsu.edu/president/docs/directives/PD\\_1997-03.pdf](http://www.sjsu.edu/president/docs/directives/PD_1997-03.pdf) requires that students with disabilities requesting accommodations must register with the [Accessible Education Center](http://www.sjsu.edu/aec) (AEC) at <http://www.sjsu.edu/aec> to establish a record of their disability.

## **Electrical Engineering Department**

### **EE Department Honor Code**

*The Electrical Engineering Department will enforce the following Honor Code that must be read and accepted by all students.*

*“I have read the Honor Code and agree with its provisions. My continued enrollment in this course constitutes full acceptance of this code. I will NOT:*

- *Take an exam in place of someone else, or have someone take an exam in my place*
- *Give information or receive information from another person during an exam*
- *Use more reference material during an exam than is allowed by the instructor*
- *Obtain a copy of an exam prior to the time it is given*
- *Alter an exam after it has been graded and then return it to the instructor for re-grading*
- *Leave the exam room without returning the exam to the instructor.”*

### ***Measures Dealing with Occurrences of Cheating***

- *Department policy mandates that the student or students involved in cheating will receive an “F” on that evaluation instrument (paper, exam, project, homework, etc.) and will be reported to the Department and the University.*
- *A student’s second offense in any course will result in a Department recommendation of suspension from the University.*

**EE174: Analog Peripheral for Embedded Systems - Tentative Course Schedule** *Subject to change with fair notice as announced by the instructor in class.*

Week	Date	Topics, Readings, Assignments, Deadlines
1	01/24	Introduction to Analog Peripheral for Embedded Systems
2	01/29	Op-Amp: Introduction
2	01/31	Op-Amp: Gain, Offset, Comparator, Schmitt trigger
3	02/05	Op-Amp: Applications
3	02/07	Experimental Lab on Op-Amp
4	02/12	Data Conversion: Sampling, Quantization
4	02/14	Data Conversion: Performance Metrics (ENOB, INL, DNL)
5	02/19	Data Conversion: Architectures (Flash, Pipeline, SAR, Oversampling)
5	02/21	Data Conversion: Signal Reconstructions (DAC)
6	02/26	Data Conversion: Experimental Lab on ADC
6	02/28	DC-DC Conversion: Concept, Charge based and Switching Regulator
7	03/05	DC-DC Conversion: Efficiency and Loading
7	03/07	Midterm 1
8	03/12	DC-DC Conversion: Experimental Lab
8	03/14	Energy Harvesting: Introduction, Basic Concepts
9	03/19	Energy Harvesting: Energy Storage, Solar Cells
9	03/21	Energy Harvesting: Experimental Lab
<b>10</b>	<b>03/26-30</b>	<b><i>Spring Recess</i></b>
11	04/02	Short Range Communications: Concepts and Needs
11	04/04	Short Range Communications: RF-ID, NFC, IEEE Standards on NFC
12	04/09	Short Range Communications: Experimental Lab
12	04/11	Phase Locking: Introduction to PLL
13	04/16	Phase Locking: Synthesizer and Clock Generators (Crystal)
13	04/18	Phase Locking: Clock and Data Recovery
14	04/23	Phase Locking: Performance Metrics (Jitter, Skew, eye-diagram opening, ...)
14	04/25	Midterm 2
15	04/30	Phase Locking: Experimental Lab
15	05/02	Display & Touch Screen: Image Sensors: LCD Display, Touch Sensor, Touch Screen
16	05/07	Display and Touch Screen: Image Sensors (CCD/CMOS)
16	05/09	Display and Touch Screen: Experimental Lab
17	05/14	Project Demo and Presentation
<b>17</b>	<b>05/16</b>	<b><i>Final Exam (2 hours 15 minutes) 19:45-22:00</i></b>