San José State University
College of Engineering, Department of Electrical Engineering
EE128, Physical Electronics, Section-01, Fall2018

Course and Contact Information

Instructor:	Lili He
Office Location:	ENG 357
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Email:	lili.he@sjsu.edu
Office Hours:	Tu Th 1:45-2:45pm
Class Days/Time:	Tu Th 10:30-11:45am
Classroom:	ENG 345
Prerequisites:	Mat 153 with "C" or better grade

Faculty Web Page and MYSJSU Messaging

Course materials include the syllabus, lecture notes, major assignment handouts, homework solutions, etc. may be found at SJSU Canvas of this course. You are responsible for regularly checking through Canvas and your MySJSU messaging information.

Course Description

The course objective is for students to be able to understand characteristics and behavior of semiconductor devices. In the process, fundamental concepts in solid-state semiconductor physics are reviewed and applied to derive current-voltage characteristics of several key semiconductor devices such as diodes, bipolar junction transistors, and metal-oxide-semiconductor field-effect transistors. Methods of device fabrication are introduced.

Course Learning Outcomes (CLO)

Upon successful completion of this course, students will be able to:

LO1 Demonstrate an understanding of the fundamentals of Electrical Engineering, including its mathematical and scientific principles, analysis and design.

LO2 Demonstrate the ability to apply the practice of Electrical Engineering in real-world problems.

LO3 Describe fundamental concepts of solid-state physics applied to the semiconductor devices.

LO4 Explain general electrical behavior of semiconductor and construct appropriate physical models.

LO5 Illustrate structural details and current-voltage characteristics of diodes, BJT, and MOSFET.

LO6 Apply the fundamental understandings of semiconductor devices with knowledge on the limitations of physical models.

Required Texts/Readings

Textbook (required) **Solid State Electronic Devices**, by Ben G. Streetman, and S. Banerjee, Prentice Hall, 7th edition, 2015. ISBN-10: 0-13-335603-5; ISBN-13: 978-13-3350603-8

Other Readings (not required)

Semiconductor Physics and Devices, Basic Principle, by Donald Neamen, 3rd Edition, McGraw-Hill, 2002

Semiconductor Device Fundamentals, by R.F. Pierret, Addison, Wesley, 1996.

Device Electronics for Integrated Circuits, by R.S. Muller and T.I. Kamins, 2nd Edition, Wiley, 1986.

Physics and Technology of Semiconductor Devices, by A.S. Grove, Wiley, 1967

Other technology requirements / equipment / material

A scientific calculator is required for homework and exam.

Course Requirements and Assignments

Assignments

There will be homework assignment about each one to two weeks depends on the length of the chapter. The assignments will be announced in class and be posted in Canvas. The deadline will be posted in the same time. Usually one week of time will be given to finish one assignment. Homework will be collected in paper in the due date in lecture time. Homework solution will be posted in Canvas after the collecting deadline. Later homework will not be accepted.
Chapter 3: One assignment
Chapter 4: One assignment
Chapter 5: Two assignments
Chapter 6: Two assignments
Chapter 7: One assignment

Exams

There are two midterm exams and one final exam. Exams cover the assigned reading materials and class lecture notes. There will be no make-up exams (only in very special circumstances, both written excuse and official proofs are required for extraordinary situations). Exam solutions will be discussed in class after the exam dates.
Success in this course is based on the expectation that students will spend, for each unit of credit, a minimum of 45 hours over the length of the course (normally three hours per unit per week) for instruction, preparation/ studying, or course related activities, including but not limited to internships, labs, and clinical practice. Other course structures will have equivalent workload expectations as described in the syllabus.

Quizzes

There will be quiz given in class time for the length of 10 minutes by the end of each chapter. Quiz normally covers the prior lecture contents.

Final Examination

Final exam is comprehensive, covering the semiconductor device portion starts from chapter 5 (Junctions) to chapter 7 (BJTs). The samples of each exam include two middle term exams and the final exam are posted in Canvas course file folder. Please check these material as the class progresses.

Grading Information

Homework	*5%*
Quiz and class participation	*10%*
Exam 1	*25%*
Exam 2	*25%*
Final exam	*35%*
Total	100%

Determination of Grades

Above 95	*A+*
90% - 94%	*A*
85% - 89%	*A-*
80% - 84%	*B+*
75% - 79%	*B*
70% - 74%	*B-*
65% - 69%	*C+*
60% - 64%	*C*
55% - 59%	*C-*
50% - 54%	*D+*
45% - 49%	*D*
40% - 44%	*D-*
below 40%	*F*

Classroom Protocol

Students are expected to participate actively in class. Students will turn their cell phones off or put them on vibrate mode while in class. They will not answer their phones in class.

Dropping and Adding

Students are responsible for understanding the policies and procedures about add/drops, academic renewal, etc. Information on add/drops are available at http://info.sjsu.edu/web-dbgen/narr/soc-fall/rec-298.html. Information about late drop is available at http://www.sjsu.edu/sac/advising/latedrops/policy/ **.** Students should be aware of the current deadlines and penalties for adding and dropping classes.

University Policies

Academic integrity

Students should know that the University's Academic Integrity Policy is availabe at http://www.sa.sjsu.edu/download/judicial_affairs/Academic_Integrity_Policy_S07-2.pdf. Your own commitment to learning, as evidenced by your enrollment at San Jose State University and the University's integrity policy, require you to be honest in all your academic course work. Faculty members are required to report all infractions to the office of Student Conduct and Ethical Development. The website for Student Conduct and Ethical Development is available at http://www.sa.sjsu.edu/judicial_affairs/index.html.

Instances of academic dishonesty will not be tolerated. Cheating on exams or plagiarism (presenting the work of another as your own, or the use of another person's ideas without giving proper credit) will result in a failing grade and sanctions by the University. For this class, all assignments are to be completed by the individual student unless otherwise specified. If you would like to include in your assignment any material you have submitted, or plan to submit for another class, please note that SJSU's Academic Policy F06-1 requires approval of instructors.

Campus Policy in Compliance with the American Disabilities Act

If you need course adaptations or accommodations because of a disability, or if you need to make special arrangements in case the building must be evacuated, please make an appointment with me as soon as possible, or see me during office hours. Presidential Directive 97-03 requires that students with disabilities requesting accommodations must register with the DRC (Disability Resource Center) to establish a record of their disability.

EE Department Honor Code

The Electrical Engineering Department will enforce the following Honor Code that must be read and accepted by all students.
"I have read the Honor Code and agree with its provisions. My continued enrollment in this course constitutes full acceptance of this code. I will NOT:
- *Take an exam in place of someone else, or have someone take an exam in my place*
- *Give information or receive information from another person during an exam*
- *Use more reference material during an exam than is allowed by the instructor*
- *Obtain a copy of an exam prior to the time it is given*
- *Alter an exam after it has been graded and then return it to the instructor for re-grading*
- *Leave the exam room without returning the exam to the instructor."*

Measures Dealing with Occurrences of Cheating

- *Department policy mandates that the student or students involved in cheating will receive an "F" on that evaluation instrument (paper, exam, project, homework, etc.) and will be reported to the Department and the University.*
- *A student's second offense in any course will result in a Department recommendation of suspension from the University.*

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Course Schedule: *Schedule is tentative and subject to change*

Week	Date	Topics	Readings
1	8/21	Class logistics, review of semiconductor concepts	Chapter 3: 3.1-3.2
2	8/28, 8/30	Fermi distribution; Carrier concentration; Drift in semiconductor	Chapter 3: 3.3-3.4
3	9/4, 9/6	Excess carriers in semiconductors	Chapter 4: 4.1-4.4;
4	9/11, 9/13	P-N Junctions: Fabrication; equilibrium conditions	Chapter 5: 5.1-5.2;
5	9/18, 9/20	P-N Junctions: p-n junction operation; steady state	Chapter 5: 5.3.-5.4 (5.4.1-5.4.2)
6	9/25, 9/27	P-N Junctions: reverse break down, transient and A-C conditions, deviation from simple theory, M/S and Hetero-junctions	Chapter 5: 5.5 (5.5.1-5.5.3)-5.6 Chapter 5: 5.7-5.8
7	10/2, 10/4	Review for 1st exam, **1st Mid-Exam 10/4/2018**	
8	10/9, 10/11	Exam results discussion, MOS Fundamentals: transistor operation, the MIS FET	Chapter 6: 6.1, and 6.4.1
9	10/16, 10/18	MOS Fundamentals: MOS capacitor	Chapter 6: 6.4.2-6.4.5
10	10/23, 10/25	MOS FET: MOSFET Operation	Chapter 6: 6.5.1-6.5.7
11	10/30, 11/1	MOS Characteristics	Chapter 6: 6.5.8-6.5.12
12	11/6, 11/8	Review for 2ne exam, **2nd Mid-Exam 11/8/2018**	
13	11/13, 11/15	Exam results discussion, MOS Characteristics; Bipolar Transistor Fundamentals:	Chapter 7: 7.1-7.3
14	11/20, 11/22	Terminal currents, Thanksgiving Recess in 11/22.	Chapter 7: 7.4
15	11/27, 11/29	BJT terminal currents; Generalized biasing	Chapter 7: 7.4
16	12/4, 12/6	BJT other effects, HBT 12/6 last day of instruction, review for final.	Chapter 7:7.5-7.7
Final Exam	**12/12/2018**	**Wednesday, 12/12/2018, 9:45-12:00pm**	