Coordinator: Dr. Hiu Yung Wong
Instructor: Ajay Mysore Nataraj
Office Location: ENG 258
Email: ajay.mysorenataraj@sjsu.edu
Office Hours: By Appointment
Lab Day/Time: Tuesday, 1:30PM - 4:15PM
Lab room: Engineering Building, room E258
Prerequisites: EE122, and EE128 with grades of C or better
Knowledge of building the circuit in LTspice

Course Description
EE 124 Laboratory is part of the EE 124 course. Students taking EE 124 are required to register for one lecture section and one laboratory section. At the end of the semester, laboratory work will be integrated with the lecture part to determine EE 124 course grade. Students must complete the laboratory in order to complete EE124 course. Major activities of EE124 laboratory are listed as below:
− Understanding the operation of the analog circuits using LTspice simulations
− Design and Implementation of analog circuits and analysis of the output using oscilloscopes and multimeters
− Develop python program for the automation of the signal generation and analysis
− Prepare weekly report
Required Lab Manual

Laboratory handouts and documents will be distributed as soft-copies in Canvas (for students to download).

Laboratory Protocol

● You are required to attend every lab meeting and your attendance is mandatory (see “Determination of Grades” section)
● If you’re unable to attend any of the labs then you should coordinate with TA.
● Labs sessions cannot be switched, with some exceptions due to unavoidable circumstances
● If you fail to attend any lab then you won’t be allowed to submit a report on that lab.

Lab Computers

● The computers in the laboratory will be used for many lab sections and data disks may be re-formatted at any time, DO NOT store your files on the lab computers.
● You will be assigned your PC and a seat in the first lab session. DO NOT use another student’s computer throughout the semester.
● Each time when you log in to a new computer, an environment will be built for you on that computer. So, each student should use one particular computer throughout the semester.
● To organize and save your data on the lab computer, create your own parent folder by your name (example, Clint_Eastwood in the Google drive) and save all your data in this parent folder.
● You shall be responsible for the costs of repairing the damage caused. You should make reasonable efforts to use laboratory instruments carefully.

Laboratory Exercise Reports

The format for the laboratory exercise report will be posted on Canvas. Each laboratory exercise report must be turned in as scheduled. Students may be asked to demonstrate their lab exercises anytime so please make sure that data and programs are always available. Each
student is responsible for individual laboratory exercise reports. (see “Determination of Grades” section)

University Policies

Academic integrity

Your commitment as a student to learning is evidenced by your enrollment at San Jose State University. The University’s Academic Integrity policy, located at http://www.sjsu.edu/senate/policies/pol_plagarism_acad_integrity/index.html, requires you to be honest in all your academic course work. Faculty members are required to report all infractions to the office of Student Conduct and Ethical Development. The Student Conduct and Ethical Development website is available at http://www.sjsu.edu/studentconduct/

Instances of academic dishonesty will not be tolerated. Cheating on exams or plagiarism (presenting the work of another as your own, or the use of another person’s ideas without giving proper credit) will result in a failing grade and sanctions by the University. For this class, all assignments are to be completed by the individual student unless otherwise specified. If you would like to include your assignment or any material you have submitted or plan to submit for another class, please note that SJSU's Academic Policy S07-2 requires the approval of instructors.

Campus Policy in Compliance with the American Disabilities Act

If you need course adaptations or accommodations because of a disability, or if you need to make special arrangements in case the building must be evacuated, please make an appointment with me as soon as possible, or see me during office hours. Presidential Directive 97-03 requires that students with disabilities requesting accommodations must register with the Accessible Education Center (AEC) at http://www.sjsu.edu/aec/ to establish a record of their disability.

EE Honor Code - Honesty and Respect for Others and Public Property

The Electrical Engineering Department will enforce the following Honor Code that must be read and accepted by all students.
“I have read the Honor Code and agree with its provisions. My continued enrollment in this course constitutes full acceptance of this code. I will NOT:

- Take an exam in place of someone else, or have someone take an exam in my place
- Give information or receive information from another person during an exam
- Use more reference material during an exam that is allowed by the instructor
- Use information, programs/codes from other students for my lab/project reports
- Allow someone else to do lab and/or project for me
- Give other students my lab information, data, programs/codes, reports, or do the labs/project for other students
- Obtain a copy of an exam prior to the time it is given
- Alter an exam after it has been graded and then return it to the instructor for re-grading
- Leave the exam room without returning the exam to the instructor.”

Measures Dealing with Occurrences of Cheating

- Department policy mandates that the student or students involved in cheating will receive an “F” on that evaluation instrument (paper, exam, project, homework, etc.) and will be reported to the Department and the University.
- A student’s second offense in any course will result in a Department recommendation of suspension from the University.

Grading Information

The lab exercises and the final project together with the lecture exams and homework assignments make up EE 124 course grade. Eight (8) laboratory exercises with reports and demos: 25%

Determination of Grades

- Every lab has equal weight (totally 25% of the final score). Lab report constitutes 50% of the lab score (lab report score) and lab attendance constitutes another 50% (lab attendance score). Students must attend at least 2 hours in each lab to receive full lab attendance score. Attending less than 2 hours will receive a prorated score (e.g. attending 1 hour will receive 50% of the lab attendance score). Students still get full lab
attendance score even they attend less than 2 hours if they can demonstrate to TA they have completed the lab.

- Lab reports must be submitted on time to receive full credit. Late submission: Half of the credit will be given if submitted within 3 days after the due date. No credit will be given if submitted after late submission due dates

**Laboratory Schedule (tentative)**

*Schedule and the content of lab assignments are subject to change with fair notice by email and class announcement*

<table>
<thead>
<tr>
<th>Week</th>
<th>Date</th>
<th>Lab</th>
<th>Report</th>
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<tbody>
<tr>
<td>1</td>
<td>29-Jan</td>
<td>Lab 1: &quot;WEEK 1: SPICE Modeling of OpAmp&quot;</td>
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<tr>
<td>2</td>
<td>5-Feb</td>
<td>Lab 2: &quot;WEEK 2: Physical Verification of OpAmp&quot;</td>
<td>Report 1 due</td>
</tr>
<tr>
<td>3</td>
<td>12-Feb</td>
<td>Lab 3: &quot;WEEK 3/4: Test Automation with Python&quot;</td>
<td>Report 2 due</td>
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<tr>
<td>4</td>
<td>19-Feb</td>
<td>Lab 4: &quot;WEEK 5: MOS Cascode and Current Mirrors&quot;</td>
<td>Report 3 due</td>
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<tr>
<td>5</td>
<td>26-Feb</td>
<td>Lab 5: &quot;WEEK 6/7: MOS Current Mirrors&quot;</td>
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<td>6</td>
<td>5-Mar</td>
<td>Lab 6: WEEK 8/9: Differential Pair</td>
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<td>7</td>
<td>12-Mar</td>
<td>Lab 7: WEEK 10/11: High-Frequency Modeling</td>
<td>Report 5 due</td>
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<td>8</td>
<td>19-Mar</td>
<td>No Lab</td>
<td>Report 6 due</td>
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<td>9</td>
<td>26-Mar</td>
<td>Lab 8: Design of Audio Amplifier</td>
<td>Report 7 due</td>
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<td>10</td>
<td>2-Apr</td>
<td>Lab 9: WEEK 12/13: Analog Circuits</td>
<td>Report 8 due</td>
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<td>11</td>
<td>9-Apr</td>
<td>Lab 10: WEEK 14/15: Digital Design</td>
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<td>12</td>
<td>16-Apr</td>
<td>Lab 11: WEEK 16/17: Power Electronics</td>
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<td>13</td>
<td>23-Apr</td>
<td>Lab 12: WEEK 18/19: Signal Processing</td>
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<td>14</td>
<td>30-Apr</td>
<td>Lab 13: WEEK 20/21: Image Processing</td>
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<td>15</td>
<td>7-May</td>
<td>Lab 14: WEEK 22/23: Machine Learning</td>
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