Green Sheet

**Instructor:** Prof. Tri Caohuu

**Office Location:** Engineering Building Room 375

**Telephone:** (408) 924-3925

**Email/Web:** tri.caohuu@sjsu.edu,

**Office Hours:** Mon 9:00am-10:00am, Wed 3:00pm-4:00pm (Zoom

**Class Days/Time:** Mon, Wed, 10:30am-11:45am

**Zoom Address:** TBA

**Prerequisites:** EE98 (with a grade of C or better), to be taken in parallel with EE118

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**COURSE:** EE118 Lab - Digital Logic Circuit Design Laboratory (online)

Coordinated by Prof. Caohuu, and taught by

EE118-02: Tue, 1:30 pm - 4:15pm, Virtual, taught by
Tri Caohuu

EE118-03: Thu, 1:30 pm - 4:15 pm, Virtual, taught by
Bhautik Patel

EE118-04: Wed, noon - 2:45pm, Virtual, taught by
Tri Caohuu

**Course Outcomes:**

The goals of this laboratory course is:

1. To apply concepts and methods of digital circuit design techniques as discussed in the class (EE118) through hands-on lab modules.

2. Learn to design combinational and sequential digital systems starting from a word description that performs a set of specified tasks and functions.

3. To analyze the results of logic and timing simulations and to use these simulation results to debug digital systems.
4. Develop skills, techniques and learn state-of-the-art engineering tools (such as Verilog, Xilinx tools) to design, implement and test modern-day digital systems on FPGAs. Traditional “hard-wiring” on a breadboard using discrete (TTL) components will also be shown in appropriate labs.

5. Learning through hands-on experimentation the Xilinx tools for FPGA design as well as the basics of Verilog to design and simulate digital systems.

**CO-REQUISITE:**

EE118

**TEXTBOOK:**


**REFERENCES:**

Xilinx Vivado Design Suite 2018.3 (or earlier).

**WEB SITE:**

Class information, notices, course materials, FAQs (selected course-related e-mails between students and instructors) will be posted on the Canvas. Students are urged to visit the web site at least twice a week.

**EVALUATION:**

The weighting among lab performance, midterm, and final project

<table>
<thead>
<tr>
<th>Activity</th>
<th>Weighting</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lab report, demo, quiz, if any</td>
<td>6% for each lab</td>
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<tr>
<td>10 Experiments</td>
<td>6% for each lab</td>
</tr>
<tr>
<td>Final Project</td>
<td>25%</td>
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<tr>
<td>Midterm Project</td>
<td>15%</td>
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**EXAMS:**

There will be no exam, but “project”, which permits ample time to complete. There will be midterm and final project.

**OFFICE HOURS:**

Your lab instructor has virtual office hour to be posted.

**HELP SESSION:**

Weekly virtual help sessions will be provided by your lab instructor. The sessions will be TBA.

**Lab Report Writing Guidelines:**

Each student has to submit an e-report for each session. The main objective for the report is to communicate the results to others and to enable others to duplicate the work in a straight-forward manner.

When preparing the lab report, you should use a word processor (it will save you time to have a template that you follow for each lab, according to the guidelines described below). You have to include screen captures of all logic block diagram and schematics, simulated waveforms, and Verilog code listings. The lab report does not need to be step-by-step detailed, but should...
show that you have a good understanding of the lab. Also, the lab report should be complete, where all information requested should be in the lab report. For each lab, the listing of the report requirements will be presented during the lab lecture, and will be posted on the lab website, if necessary.

Reports are to be typed and should contain the following information. A report should be concise but thorough. The length of a typical report should not exceed 10 pages. The lab report should be uploaded on the Canvas assignment folder, promptly before due date

A. Title, date and name of the student.

B. Follow the following format

1. Pre-lab: [15 pts]
   unless otherwise indicated - these are usually given for the on-line answers/quizzes and done by each student)

   The quiz problems you tried should be listed here with answers.

2. Introduction [5 pts]

   Give the goals/objectives of the lab experiment.

3. Theory of Operation and explanation of the design [15 pts]

   Give a brief discussion of the theory of operation, including schematics and equation used, etc. This is of particular importance for the design-oriented labs. You should also explain the schematics involved in your design.

4. Experimental results:

   a. Brief description of the lab experiment. [5 pts]

   b. Schematics and Verilog code (design modules and test bench of the circuit. Put your name and date on each page. [15 pts]

   c. Simulated waveform. Photographs of working circuit on the FPGA board. Video may be included if
necessary. [20 pts]

d. Discussion of the results indicating that the circuit functions properly. It is not good enough to just give the simulated waveform and FPGA demo. For the simulated waveform, it is up to you to show that this waveform correspond to what you expect (do not just say "The simulation shows that the circuit works properly"). *You need to make it clear to the reader that the circuits work properly!* One convenient way is to give a truth table and indicate that for each entry the corresponding values given by the logic simulator by labeling the simulated waveforms. Include also a reasonable detailed discussion of the results. [10 pts]

5. Conclusion. [10 pts] unless otherwise indicated

This is an important part of the report. The conclusion should contain a summary of the results. Are the goals of the lab fulfilled? If not, explain why.

6. Sign and date

C. Neatness, organization and presentation: [5 pts]

CLASS ATTENDANCE

Attendance at lab lecture is mandatory.

For Lab use, please download the Xilinx Vivado Design Suite 2018.3 (or earlier) Webpack from the website below. Note that you must register first before downloading:

Tentative Schedule

<table>
<thead>
<tr>
<th>Module (Week)</th>
<th>Lab Activity</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 (2/01)</td>
<td>Introduction; Xilinx Vivado Design Suite download and installation, FPGA board distribution</td>
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<tr>
<td>2 (2/08)</td>
<td>Experiment A – Xilinx Vivado Design Suite Tools; Basic HDL Design Entry &amp; Simulation</td>
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<tr>
<td>Date</td>
<td>Experiment</td>
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<tr>
<td>3 (2/15)</td>
<td>Experiment B – Xilinx Vivado Design Suite; Advanced HDL programming &amp; behavioral simulation.</td>
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<tr>
<td>4 (2/22)</td>
<td>Experiment C - Overview of FPGA architecture, Synthesis, implementation, timing simulation and demonstration on FPGA board.</td>
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<td>5 (3/01)</td>
<td>Experiment D – Design and simulation of various comparators.</td>
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<tr>
<td>6 (3/08)</td>
<td>Experiment E – Design and simulation and FPGA demonstration of multipliers</td>
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<tr>
<td>3/15</td>
<td>Midterm project assignment and demonstration</td>
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<td></td>
<td>Submission Duration: 2 weeks (April 1)</td>
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<td>7 (3/22)</td>
<td>Experiment F – Flip-flops: Simulation</td>
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<td>Submission duration: 2 weeks (April 8)</td>
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<td>8 (3/29)</td>
<td>Spring Recess</td>
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<td>9 (4/05)</td>
<td>Experiment G – Design, simulation, and FPGA demonstration of BCD counters</td>
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<td>Submission duration: 2 weeks (22 April)</td>
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<tr>
<td>10 (4/12)</td>
<td>Experiment H – Design, simulation, and FPGA demonstration of finite state machines (FSM)</td>
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<td>Submission duration: 2 weeks (29 April)</td>
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<td>11 (4/19)</td>
<td>Experiment I – Design, simulation, and FPGA demonstration of Arithmetic Logic Unit</td>
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<td>Submission Duration: 2 weeks (6 May)</td>
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<tr>
<td>4/26</td>
<td>Final Project Demonstration and report submission</td>
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<td>Submission Duration: 2.5 weeks (17 May)</td>
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**Additional Rules for Spring 2021 EE Laboratories**
Component Pickup Procedure

- Necessary components and devices will be provided to students by the department.

- Students living within a 60 miles radius from campus will receive a designated time to pick up their components.

- Those living further than 60 miles can have their components and/or devices mailed in which a return label will be included.

- Prior to picking up or mailing, students must fill out the Docusign form including the designated receiver’s information.

- If a student would like to designate someone else to pick up on behalf of them, there will be an option on the Docusign.

- In the case components are lost or broken, students must contact the department as soon as possible to avoid an incomplete grade and/or registration hold.

- Students will have to come on campus a second time to pick up the ADALM 2000 should a course requires it. Unfortunately, the shipment for the devices will arrive sometime after school has begun.

Dropping Course after Receiving Components

- Students must return components to the EE department either in person or through mail using the provided return label.

- Components and devices must be in the office by Feb 15th to avoid an incomplete grade and/or registration hold.

Adding a Course

- If a student has completed a Docusign form for a course, but components have not been picked up/mailed yet, and they choose to add another course, an email can be sent to ee-techsupport-group@sjsu.edu to amend their previous form.

- If a student has their components or devices already, an additional Docusign form will need to be submitted prior to adding a new course.

- If multiple courses need to be added, students need to wait until enrolled before submitting one Docusign for all the courses.
• Please submit these forms prior to Feb 15th to receive new components or devices.

Returning Components and Devices

• Detailed instructions on returning procedure will be provided to students later in the semester.

• Students need to return components and devices in working condition to avoid an incomplete grade and/or registration hold.

• Course of action will be discussed on a case by case basis for any broken or missing components at the time of return.

• Components and devices need to be returned no later than May 17th.

• Please plan to drop off or mail components at an appropriate time, as those returned past the deadline will not be accepted and will result in an incomplete grade and/or registration hold.

Code of conduct while in labs on campus (not applicable to EE118 Lab Spring 2021)

• Students attending in-person labs are required to wear face coverings, regularly sanitize/wash hands, and maintain 6 feet (about 2 arms' length) distance between each other at all times while in the building. Check SJSU Health Advisories website for updated information about university requirements and rules https://www.sjsu.edu/healthadvisories/

• Students need to check with the lab instructor about the process to get on campus.

• Students must only work in designated stations at all times.

• Disposable masks will be provided if forgotten.

• If attending in person lab 2 days in a row, washed/clean cloth masks or new disposable masks must be worn each day.

• Disinfecting wipes are provided in each lab, and students are expected to wipe down their stations before and after each use.

• Students are strongly encouraged to bring a personal mouse or keyboard to avoid using shared devices.
• Please keep in mind drinking fountains are not available, so plan accordingly.