For Lab use, please download the Xilinx ISE Design Suite 14.7 Webpack from the website below. Note that you must register first before downloading.


<table>
<thead>
<tr>
<th>Session Number</th>
<th>Week of</th>
<th>Lab Activity (Pre-Lab work is required!)</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Jan. 30</td>
<td>Introduction</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>Feb. 6</td>
<td>Experiment A – Xilinx ISE Tools; Schematic Entry &amp; Simulation</td>
<td>Simple to moderately complex design schematic entry &amp; simulation</td>
</tr>
<tr>
<td>3</td>
<td>Feb. 13</td>
<td>Experiment B – Xilinx ISE Tools HDL &amp; Simulation</td>
<td>Simple to moderately complex design HDL coding &amp; simulation</td>
</tr>
<tr>
<td>4</td>
<td>Feb. 20</td>
<td>Experiment C – Familiarization of TTL ICs (Parts I &amp; II)</td>
<td>Familiarization of TTL ICs</td>
</tr>
</tbody>
</table>

**Tentative Lab Schedule**
<table>
<thead>
<tr>
<th>Week</th>
<th>Date</th>
<th>Experiment</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>Feb.27</td>
<td>Experiment D – Hard-wiring of 2-bit comparator</td>
<td>Building a circuit on a breadboard</td>
</tr>
<tr>
<td>6</td>
<td>Mar.5</td>
<td>Experiment E – Schematic Entry, Simulation and <a href="#">FPGA Demonstration</a> of the 2-bit Comparators</td>
<td>Repeat the design using FPGA</td>
</tr>
<tr>
<td>7</td>
<td>Mar.12</td>
<td>Midterm</td>
<td>Part I: Written</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Part II: Demo</td>
</tr>
<tr>
<td>8</td>
<td>Mar.19</td>
<td>Experiment F – 4-Bit Comparator: Verilog modeling (hierarchical), simulation, synthesis, and demo on FPGA board</td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>Mar.26</td>
<td>Experiment G – Flip-Flops: Simulation (Part 1)</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>Apr.2</td>
<td>Experiment G – Flip-Flops: Simulation (Part 2)</td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>Apr.9</td>
<td>Experiment H – BCD Counter Design and Hardwiring</td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>Apr.16</td>
<td>Experiment I – Design &amp; Demo of HEX Counter Using Artix FPGA Board</td>
<td></td>
</tr>
<tr>
<td>13</td>
<td>Apr.23</td>
<td>Experiment J – Traffic Light Controller (FF-based, “Richards Controller”-based, or Verilog/FPGA)</td>
<td></td>
</tr>
<tr>
<td>14</td>
<td>Apr.30</td>
<td>Final Project</td>
<td>Part I: Written</td>
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<tr>
<td></td>
<td></td>
<td></td>
<td>Part II: Demo</td>
</tr>
</tbody>
</table>
EE118 Lab - Digital Logic Circuit Design Laboratory (ENG305)

Coordinated by Prof. Tri Caohuu, and taught by

**COURSE:**

EE118-02: Tue, 1:30 pm-4:15 pm, ENG-305(Lab), taught by Nivedita Shiva Murthy

EE118-03: Thu, 1:30 pm-4:15 pm, ENG-305(Lab), taught by Arjav Dave

EE118-04: Wed, Noon-2: 45 pm, ENG-305(Lab), taught by Shanmathi Saravanan

The goals of this laboratory course is:

1. To apply concepts and methods of digital circuit design techniques as discussed in the class (EE118) through hands-on lab modules. [a]

2. Learn to design combinational and sequential digital systems starting from a word description that performs a set of specified tasks and functions. [c]

3. To analyze the results of logic and timing simulations and to use these simulation results to debug digital systems. [b]

4. Develop skills, techniques and learn state-of-the-art engineering tools (such as Verilog, Xilinx tools) to design, implement and test modern-day digital systems on FPGAs. Traditional “hard-wiring” on a breadboard using discrete (TTL) components will also be practiced in appropriate labs [i]

5. Learning through hands-on experimentation the Xilinx tools for FPGA design as well as the basics of Verilog to design and simulate digital systems. [k]

**CO-REQUISITE:**

REFERENCES: Xilinx, ISE Student Edition 14.7, (Xilinx schematic capture and simulation software; Lab PCs have this software installed. Also maybe downloaded from Xilinx website.).

WEB SITE: Class information, notices, course materials, FAQs (selected course-related e-mails between students and instructors) will be posted on the Canvas. In addition, all the changes on the tentative list of homework problems (see below), as well as solutions to homework, will be available on the web. Students are urged to visit the web site at least twice a week.

The weighting among lab performance, midterm, and final project

Lab report, demo & pre-lab report, quiz, if any
- 60 % for Report Submissions (10 Lab sessions)

EVALUATION: - 10% of Quizzes
- 15% of Midterm
- 25% of Final exam/project

EXAMS: There will be a midterm and a final exam or project in the lab.

OFFICE HOURS: Your lab instructor has office hours posted.

HELP SESSION: Weekly help sessions will be provided by your lab instructor. The sessions will be TBA in IEEE Room.
Each student has to submit a report for each session. The main objective of the report is to communicate the results to others and to enable others to duplicate the work in a straight-forward manner.

When preparing the lab report, you should use a word processor (it will save you time to have a template that you follow for each lab, according to the guidelines described below). You have to include printouts of all logic schematics, simulated waveforms, and Verilog code listings if any. The lab report does not need to be step-by-step detailed but should show that you have a good understanding of the lab. Also, the lab report should be complete, where all the information requested should be in the lab report. For each lab, the listing of the report requirements will be presented during the lab lecture and will be posted on the lab website, if necessary.

Reports are to be either neatly hand-written or, preferably, typed (or a combination of both) and should contain the following information. A report should be concise but thorough. The length of a typical report should not exceed 10 pages. The lab report is due at the start of the next lab.

1. Cover Page

2. Follow the following format (The report counts for 90 points out of a total of 100 points per lab)

**Pre-lab:** (10 points, to be submitted online via canvas before each respective lab experiment, 3-5 pages)

Prelab Report Format:

- Cover Page (Title, date, and name of the student, Instructor's name)
- Introduction/Background
- Goal of the experiment
- Relevant Diagrams

**Lab Report Format:**

1. **Cover Page** *(Title, date, and name of the student, Instructor's name)*

2. **Introduction/Background** *(15 Points)*

Give a brief discussion of the theory of operation, including schematics and equations used, etc. This is of particular importance for the design-oriented labs. You should also explain the schematics involved in your design.
3. Goal of the Experiment (10 Points)

Give the goals/objectives of the lab experiment.

4. Procedure (if any) (20 Points)

5. Results and Discussion (25 Points)

a. Simulated waveform/resulting circuit (snapshots).

b. Discussion of the results indicating that the circuit functions properly. It is not good enough to just give the simulated waveform. It is up to you to show that this waveform corresponds to what you expect (do not say "The simulation shows that the circuit works properly"). You need to make it clear to the reader that the circuits work properly! One convenient way is to give a truth table and indicate that for each entry the corresponding values given by the logic simulator by labeling the simulated waveforms. Include also a reasonably detailed discussion of the results.

5. Conclusion (15 Points)

This is an important part of the report. The conclusion should contain a summary of the results. Are the goals of the lab fulfilled? If not, explain why.

- Neatness, organization, and presentation: 5 points
"I have read the Honor Code and agree with its provisions. My continued enrollment in this course constitutes full acceptance of this code. I will NOT:

- Take an exam in place of someone else, or have someone take an exam in my place
- Give information or receive information from another person during an exam
- Use more reference material during an exam than is allowed by the instructor
- Obtain a copy of an exam prior to the time it is given
- Alter an exam after it has been graded and then return it to the instructor for re-grading
- Leave the exam room without returning the exam to the instructor."

**Measures Dealing with Occurrences of Cheating**

- Department policy mandates that the student or students involved in cheating will receive an “F” on that evaluation instrument (paper, exam, project, homework, etc.) and will be reported to the Department and the University.

- A student’s second offense in any course will result in a Department recommendation of suspension from the University.

**EE HONOR CODE**

In addition to EE Honor Code, EE118 students understand that professional attitude is necessary to maintain a comfortable academic environment. For examples:

- I do not just skip the lecture and then ask the instructor to summarize the lecture for me later on.

**Office hours are for students to have questions, not for the instructor to summarize the lecture for any specific student.**

- I come to the class on time and leave the class at the end of the lecture.
- To minimize possible tension during the exams, I WILL follow the exam rules closely.
- I work on the lab assignments and the final project by myself.
- I understand that long-term learning is my responsibility and so I always keep it up.
- I strongly believe that NOT any statement similar to examples below can be used:
- I am working full-time and so do not have enough time for the class.
- I have quite many classes this semester and so I do not have enough time for the class.
- I just need a passing grade to graduate this semester.
• I live far away from the campus and so I can not come to the class often.
• , etc....