EE118 **FALL 2018**

SAN JOSE STATE UNIVERSITY
DEPARTMENT OF ELECTRICAL ENGINEERING

Boldness has genius, power and magic in it.
Only engage, and then the mind grows heated —
Begin it, and then the work will be completed!
(J.W. von Goethe)

Course Information (Greensheet)

COURSE:	EE118 - Digital Logic Circuit Design (aka Logic Design & Computer Organization) Lecture - Mon, Wed, 10:30am–11:45am, ENG 345 Lab - Coordinated by Prof. Choo, and taught by Lab Instructors, ENG 305
TAUGHT BY:	Prof. C. Choo, ENG 253, 924-3980, chang.choo@sjsu.edu
OBJECTIVES:	To provide a thorough background, at the introductory level, of the logical (mathematical) and electrical basis for digital (computer) system design. Major building blocks for designing digital systems will be examined and used which include gates, MUXes, DEMUXes, decoders, encoders, comparators, various arithmetic blocks, flip-flops, counters, registers, RAMs/ROMs, PLDs and FPGAs. The course will conclude with designing a simple computer CPU consisting of all the components covered throughout the semester. Students will also learn to design digital circuits using schematic and Hardware Description Language (HDL), particularly, Verilog. This course is the gateway to all other digital embedded and computer system design courses in the curriculum.
ABET-Compliant Learning Objectives/Outcomes:	1) The ability to understand the number system, including binary, octal and hexadecimal numbers, and 2's complement number representation. 2) The ability to understand Boolean algebra and to apply various Boolean theorems to prove Boolean identities and to simplify Boolean functions. 3) The ability to understand the transistor-level structure of TTL and CMOS logic gates and their electrical and timing characteristics. 4) The ability to construct the K-map from a Boolean expression and to find the minimal SOP/POS forms.

5) The ability to understand basic concept of Quine-McCluskey algorithm, i.e., to construct the Q-M table, to perform matching iterations to find PIs, and to find essential PIs by either detecting dominance relations or using Patrick function to corresponding Boolean expression.
6) The ability to design moderately complex arithmetic and logic circuits including carry lookahead adder, BCD adder, comparator, multiplier, and to evaluate the resulting performance in terms of gate count and propagation delay.
7) The ability to understand the working of MSI devices including decoders, encoders, and multiplexers, and to design various logic circuits using them.
8) The ability to analyze cross-coupled gates and to identify any metastability.
9) The ability to understand the behavior, timing issues, and internal structure of various flip-flops (RS, JK, D and T) and registers.
10) The ability to identify and prevent various hazard and timing problems.
11) The ability to analyze and design various flip-flop-based state machines (synchronous sequential circuits), including counters and one-hot controller.
12) The ability to understand how PLA, ROM, and modern FPGA work and how to use them to design complex logic circuits, including a simple CPU.
13) The ability to understand the basics of HDL language, to write a HDL program for various logic circuits and to test their functionality and timing.
14) The ability to use CAD software, tools, and instruments to design, debug, test, and evaluate the performance of various logic circuits.
15) The ability to work in a group. In the lab, students are typically divided into 2-person groups. All lab modules, except the final project, are group efforts graded as a team.
16) The ability to prepare technical documents. There are a number of lab modules in this course. Students are required to submit a comprehensive lab report for each lab module. Lab reports are graded both for technical content and presentation.

PREREQUISITE: EE98 (with a grade of C or better)

TEXTBOOK: C.Y. Choo, Digital Logic Design, Manuscript, January 2011 (Draft 7.0). Available from Maple Press, 481 E. San Carlos St. between 10th and 11th St. (Tel:408-297-1000)

REFERENCES: J.F. Wakerly, Digital Design: Principles and Practices, 4th ed., Prentice Hall, 2006
(A former textbook. A comprehensive textbook with many practical and advanced design problems).

M.M. Mano, Digital Design, 3rd ed., Prentice Hall, 2002 (One of the "student-friendly" textbooks for its plain style).

R.H. Katz, Contemporary Logic Design, Benjamin/Cummings, 1994 (One of former textbooks in SJSU).

E.L. Johnson and M.A. Karim, Digital Design: A Pragmatic Approach, PWS-Kent, 1987 (Contains an excellent list of suggested readings for further study at the end of each chapter; out of print unfortunately).

F. J. Hill and G. R. Peterson, Introduction to Switching Theory and Logical Design, 3rd ed., John Wiley & Sons, 1981 (A classical textbook. Your professors used this book when they were students.).

Xilinx, ISE Web Edition 8.2i or higher, (Xilinx schematic capture and simulation software; Lab PCs have this software installed, with Modelsim attached) http://www.xilinx.com/webpack/classics/wpclassic/index.htm).

Altera, Quartus II Version 11.1 or higher Web Edition Software (may be downloaded from Altera web site; schematic, Modelsim verilog, and VHDL simulation).

WEBSITE:

Class information, notices, course materials, FAQs (selected course-related e-mails between students and instructors) will be posted on the web: SJSU Canvas. In addition, all the changes on the tentative list of homework problems (see below), as well as solutions to homework, will be available on the web. Students are urged to visit the web site at least twice a week.

EVALUATION (ABET-Compliant In-Class Assessment):

The weighting among exams, assignments, and laboratory will be:

Laboratory	25%
Three Midterms	15% × 3
Final	25%
Homework	5%

All 3 midterm exams should be taken.

EXAMS:

Please note the following exam schedules:

Exam I Mon, Sep.24, in-class

Exam II	Mon, Oct.29, in-class
Exam III	Mon, Nov.26, in-class
Final	Tue, Dec.18, 9:45am-noon, in-class

Students are responsible for adjusting their schedules to take these exams at these times. Make-up exams will *not* be given except in the case of extraordinary circumstances (such as death of a family member or significant traffic accident) proven with formal documents.

Exams will be closed book and closed note. No crib sheets are allowed.

GRADES: Letter grades will be given based on class and lab performance.

OFFICE HOURS: The office hours are made available for questions about lectures and assignments for discussion of grades assigned. If you need a help of the instructor, during his office hours (Wed, 9:30am-10:30am, Fri, 2:30pm-3:30pm). Use of e-mail is strongly recommended for other times, although appointments may be made for mutually convenient times.

HELP SESSION: Help sessions are provided by Grader/Assistant, TBA. The sessions will be on TBA, in IEEE Room.

~~TUTORING SESSION:~~ ~~Weekly tutoring sessions may be provided by Tutor (TBA). The sessions will be announced and will be in IEEE Room.~~

LABORATORY: Students are required to take a laboratory section concurrently with the lecture.
Administrative details of the laboratory will be given out by your lab instructor.

DROPS: After the official drop deadline, a serious and compelling reason, e.g., an extended personal illness or a death of your immediate family member, will be required to drop this course. Reasons that will *not* be valid for dropping include: low grades in the course, inadequate time to spend on the course, a change in work schedule, or a schedule conflict.

CLASS ATTENDANCE: Attendance at lecture is strongly recommended.

HOMEWORKS: Homework will be assigned weekly, except the weeks of exam, and due one week after. Solution will be posted on the web after homework reports are collected on the due date. Late homework will *not* be accepted. You may work with other students on the homework. Indeed, you are encouraged to do so. However, your report must be *original*. Homework reports

which do not meet civilized standards of appearance and presentation will be returned without grading.

Relationship to Program Objectives and ABET Program Criteria

Program objectives	Course learning objectives	Level of support
(a) an ability to apply knowledge of mathematics, science, and engineering	1-15	Advanced
(b) an ability to design and conduct experiments, as well as to analyze and interpret data	15-16	Advanced
(c) an ability to design a system, component, or process to meet desired needs	1~7	Advanced
(d) an ability to function on multi-disciplinary teams		Moderate
(e) an ability to identify, formulate, and solve engineering problems	1~8	Advanced
(f) an understanding of professional and ethical responsibility		Not supported
(g) an ability to communicate effectively	11,12	Advanced
(h) the broad education necessary to understand the impact of engineering solutions in a global and societal context		Not supported
(i) a recognition of the need for, and an ability to engage in life-long learning	10	Introductory
(j) a knowledge of contemporary issues	10	Introductory
(k) an ability to use the techniques, skills, and modern engineering tools necessary for engineering practice.	8	Advanced
(l) one or more technical specialties that meet the needs of Silicon Valley companies	1~12	Advanced

Program Criteria	Course learning objectives	Level of support
Knowledge of probability and statistics		Not supported
Knowledge of mathematics through differential and integral calculus, basic sciences, and engineering sciences necessary to analyze and design complex devices	1~7	Advanced
Systems containing hardware and software components	1~7	Advanced

Tentative Class/Lab Schedule

Lec	Date	Topics	Textbook Reading▲	Home-work Due*	Lab
1	8/22(W)	Introduction			
2	8/27(M)	Binary Logic, ICs			Lab C (Parts I & II)
3	8/29(W)	Boolean Algebra I			
4	9/5(W)	Boolean Algebra II			Lab C (cont'd)
5	9/10(M)	Combinational Circuit Analysis			Lab A/B
6	9/12(W)	K-Map		#1	
7	9/17(M)	K-Map and Quine-McCluskey Algorithm		#2	Lab D
8	9/19(W)	Number Systems, Binary Arithmetic		#3	
	9/24(M)	*Test I*			Lab E
9	9/26(W)	Hazards			
10	10/1(M)	Comparators, Multilevel Circuits			Lab F
11	10/3(W)	Decoder, Encoder			
12	10/8(M)	Multiplexer			*Midterm*
13	10/10(W)	Intro. Verilog		#4	
14	10/15(M)	Flip-Flops I			Lab G
15	10/17(W)	Flip-Flops II		#5	
16	10/22(M)	Flip-Flop III			Lab G (cont'd)
17	10/24(W)	Analysis of Synchronous		#6	

		Sequential Circuits			
	10/29(M)	*Test II*			Lab H
18	10/31(W)	Design of Synchronous Sequential Circuits			
19	11/5(M)	Counter		#7	Lab I
20	11/7(W)	Verilog for Sequential Circuits			
21	11/12(M)	Parallel and Shift Registers		#9	Lab J
22	11/14(W)	Datapath & Controller Design I			
23	11/19(M)	Dtapath & Controller Design II		#9	No Lab (Thanksgiving)
	11/26(M)	Test III			Lab K
24	11/28(W)	FPGA Architecture			
25	12/3(M)	RAM, ROM, Memory Decoding Circuits		#10	*Lab Final*
	12/5(W)	CPU Design I			
	12/10(M)	CPU Design II		#11	
	12/18(T)	*Final, 0945am-12:00pm*			

List of Tentative Homework Assignments

HW No.	Exercise Problems
1	1.1, 1.6, 2.1, 9.2, 9.6, 9.8, 8.1, 8.3, 8.4, 8.5, 8.6, 10.3
2	7.1, 7.2, 7.3, 9.1(1), 9.1(3)
3	11.1, 11.3, 11.9, Design a comparator which compares two 3-bit numbers, $A=a_2a_1a_0$ and $B=b_2b_1b_0$ and outputs G, E, and L, as in the 2-bit comparator, as discussed in class. 11.12, 11.14(1)(3), 11.15(1)(3), 11.16
4	12-2(solve only the first out of four problems),14-1(1), 14-3(2), 14-7
5	13.1, 13.3, 19.1, 19.3, 21.3(1)(2), 21.4, 21.5(1)(2), 22.1, 39-1
6	23.2, 23.7, 23.8, 20-1, 20.6, 39.3, 4-1, 4-2, 4-3, 5-1, 5-2, 5-3, 5-4
7	TBA
8	TBA
9	TBA
10	TBA
11	TBA

PLEASE DO NOT CONSUME FOOD IN THE CLASSROOM

EE@SJSU

Honesty and Respect for Others and Public Property

EE HONOR CODE

The Electrical Engineering Department will enforce the following Honor Code that must be read and
accepted by all students.
"I have read the Honor Code and agree with its provisions. My continued enrollment in this course
constitutes full acceptance of this code. I will NOT:

- *Take an exam in place of someone else, or have someone take an exam in my place*
- *Give information or receive information from another person during an exam*
- *Use more reference material during an exam than is allowed by the instructor*
- *Obtain a copy of an exam prior to the time it is given*
- *Alter an exam after it has been graded and then return it to the instructor for re-grading*
- *Leave the exam room without returning the exam to the instructor."*

Measures Dealing with Occurrences of Cheating

- *Department policy mandates that the student or students involved in cheating will receive an "F" on*
  that evaluation instrument (paper, exam, project, homework, etc.) and will be reported to the Department and the University.
- *A student's second offense in any course will result in a Department recommendation of suspension*
  from the University.

EE HONOR CODE

In addition to EE Honor Code, EE118 students understand that professional attitude is necessary to
maintain a comfortable academic environment. For examples:

- *I do not just skip the lecture and then ask the instructor to summarize the lecture for me later on.*

Office hours are for students to have questions, not for the instructor to summarize the lecture for any specific student.

- *I come to the class on time and leave the class at the end of the lecture.*
- *To minimize possible tension during the exams, I WILL follow the exam rules closely.*
- *I work on the lab assignments and final project by myself.*
- *I understand that long-term learning is my responsibility and so I always keep it up.*
- *I strongly believe that NOT any statement similarly to examples below can be used:*
- *I am working full-time and so do not have enough time for the class.*
- *I have quite many classes this semester and so I do not have enough time for the class.*
- *I just need a passing grade to graduate this semester.*
- *I live far away from the campus and so I can not come to the class often.*
- *etc., etc....*