San José State University
Electrical Engineering Department
EE118: Digital Logic Circuit Design
Section 1, Spring 2018

Course and Contact Information

Instructor:	Tan Van Nguyen
Office Location:	ENG 347A
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Email:	tan.v.nguyen@sjsu.edu
Office Hours:	MW 9:30-10:30 or by appointment
Class Code/Days/Time:	21283, MW 10:30-11:45
Classroom:	ENG 345
Prerequisites:	EE98 and EE97 with a grade of C or better. Lecture 3 hours, laboratory 3 hours. 4 units.
Laboratory:	Students are required to take a laboratory section concurrently with the lecture. Administrative details of the laboratory will be given out by your lab instructor.

Faculty Web Page

Course materials such as syllabus, handouts, lecture notes, lab assignment instructions and homework can be found on my faculty web page at http://www.sjsu.edu/people/tan.v.nguyen/courses.

Class information, notices, course materials, FAQs (selected course-related e-mails between students and instructors) will be posted on Canvas. In addition, all the changes on the tentative list of homework problems (see below), as well as solutions to homework, will be available on Canvas. Students are urged to visit the web site at least twice a week.

Course Objectives

To provide a thorough background, at the introductory level, of the logical (mathematical) and electrical basis for digital (computer) system design. Major building blocks for designing digital systems will be examined and used which include gates, MUXes, DEMUXes, decoders, encoders, comparators, various arithmetic blocks, flip-flops, counters, registers, RAMs/ROMs, PLDs and FPGAs. The course will conclude with designing a simple computer CPU consisting of all the components covered throughout the semester. Students will also learn to design digital circuits using schematic and Hardware Description Language (HDL), particularly, Verilog. This course is the gateway to all other digital embedded and computer system design courses in the curriculum.

ABET-Compliant Learning Objectives/Outcomes

1) The ability to understand the number system, including binary, octal and hexadecimal numbers, and 2's complement number representation.
2) The ability to understand Boolean algebra and to apply various Boolean theorems to prove Boolean identities and to simplify Boolean functions.
3) The ability to understand the transistor-level structure of TTL and CMOS logic gates and their electrical and timing characteristics.
4) The ability to construct the K-map from a Boolean expression and to find the minimal SOP/POS forms.
5) The ability to understand basic concept of Quine-McCluskey algorithm, i.e., to construct the Q-M table, to perform matching iterations to find PIs, and to find essential PIs by either detecting dominance relations or using Patrick function to corresponding Boolean expression.
6) The ability to design moderately complex arithmetic and logic circuits including carry lookahead adder, BCD adder, comparator, multiplier, and to evaluate the resulting performance in terms of gate count and propagation delay.
7) The ability to understand the working of MSI devices including decoders, encoders, and multiplexers, and to design various logic circuits using them.
8) The ability to analyze cross-coupled gates and to identify any metastability.
9) The ability to understand the behavior, timing issues, and internal structure of various flip-flops (RS, JK, D and T) and registers.
10) The ability to identify and prevent various hazard and timing problems.
11) The ability to analyze and design various flip-flop-based state machines (synchronous sequential circuits), including counters and one-hot controller.
12) The ability to understand how PLA, ROM, and modern FPGA work and how to use them to design complex logic circuits, including a simple CPU.
13) The ability to understand the basics of HDL language, to write a HDL program for various logic circuits and to test their functionality and timing.
14) The ability to use CAD software, tools, and instruments to design, debug, test, and evaluate the performance of various logic circuits.
15) The ability to work in a group. In the lab, students are typically divided into 2-person groups. All lab modules, except the final project, are group efforts graded as a team.
16) The ability to prepare technical documents. There are a number of lab modules in this course. Students are required to submit a comprehensive lab report for each lab module. Lab reports are graded both for technical content and presentation.

Required Textbook

C.Y. Choo, Digital Logic Design, Manuscript, August 2014 (Draft 7.2). Available from Maple Press, 330 S 10th St. #200. (Tel:408-297-1000)

References

1) J.F. Wakerly, Digital Design: Principle and Practices, 4th Edition, Prentice Hall, 2006 (A former text book. A comprehensive text book with many particle and advanced design problems).
2) M.M. Mano, Digital Design, 3rd Edition, Prentice Hall, 2002 (One of the "student-friendly" text book for its plain style).
3) R.H. Katz, Contemporary Logic Design, Benjamin/Cummings, 1994 (One former textbooks in SJSU).
4) F. J. Hill and G. R. Peterson, Introduction to Switching Theory and Logical Design, 3rd Edition, John Wiley & Sons, 1981 (A classical textbook. Your professors used this book when they were students).

5) Xilinx, ISE Web Edition 8.2i or higher, (Xilinx schematic capture and simulation software; Lab PCs have this software installed, with Modelsim attached) http://www.xilinx.com/webpack/classics/wpclassic/index.htm).

Course Requirements and Assignments

SJSU classes are designed such that in order to be successful, it is expected that students will spend a minimum of forty-five hours for each unit of credit (normally three hours per unit per week), including preparing for class, participating in course activities, completing assignments, and so on. More details about student workload can be found in University Policy S12-3 at http://www.sjsu.edu/senate/docs/S12-3.pdf.

Other course structures will have equivalent workload expectations as described in the syllabus.

Evaluation

The weighting among exams, assignments, and laboratory will be:

Laboratory	25%
Homework/Quizzes	5%
Two Midterms	20% each
Final Exam	30%

Examination

Please note the following exam schedules:

EXAM I: March 05th
EXAM II: April 18th
FINAL EXAM: May 21st, 2018 from 09:45 to 12:00

Students are responsible for adjusting their schedules to take these exams at these times. Make-up exams will *not* be given except in the case of extraordinary circumstances (such as death of a family member or significant traffic accident) proven with formal documents.

Exams will be closed book and closed note. No crib sheets are allowed.

Grading Policy

There will be no make-up exams/quizzes and those absent will receive no credit. Students must write their answers clearly in an organized fashion. Further instructions will be provided during exams. This course must be passed with a C or better as a CSU graduation requirement.
Letter grades will be given based on class and lab performance.

Help/Tutoring Session

Help sessions are provided by Grader/Assistant, TBA. The sessions will be on TBA, in IEEE Room.

Tutoring Session

Weekly tutoring sessions may be provided by Tutor (TBA). The sessions will be announced and will be in IEEE Room.

Classroom Protocol

Arrive on time, no food in class or lab, turn off cell phone, NO private discussion in class.

Class Attendance

Attendance at lecture is strongly recommended.

Homework/Quizzes
Homework will be assigned weekly, except the weeks of exam, and due one week after. Solution will be posted on the web after homework reports are collected on the due date. Late homework will *not* be accepted. You may work with other students on the homework. Indeed, you are encouraged to do so. However, your report must be *original*. Homework reports which do not meet civilized standards of appearance and presentation will be returned without grading. Quizzes will be announced in class.

University Policies

General Expectations, Rights and Responsibilities of the Student
As members of the academic community, students accept both the rights and responsibilities incumbent upon all members of the institution. Students are encouraged to familiarize themselves with SJSU's policies and practices pertaining to the procedures to follow if and when questions or concerns about a class arises. See University Policy S90–5 at http://www.sjsu.edu/senate/docs/S90-5.pdf. More detailed information on a variety of related topics is available in the SJSU catalog, at http://info.sjsu.edu/web-dbgen/narr/catalog/rec-12234.12506.html. In general, it is recommended that students begin by seeking clarification or discussing concerns with their instructor. If such conversation is not possible, or if it does not serve to address the issue, it is recommended that the student contact the Department Chair as a next step.

Dropping and Adding
Students are responsible for understanding the policies and procedures about add/drop, grade forgiveness, etc. Refer to the current semester's Catalog Policies section at http://info.sjsu.edu/static/catalog/policies.html. Add/drop deadlines can be found on the current academic year calendars document on the Academic Calendars webpage at http://www.sjsu.edu/provost/services/academic_calendars/. The Late Drop Policy is available at http://www.sjsu.edu/aars/policies/latedrops/policy/**.** Students should be aware of the current deadlines and penalties for dropping classes. Information about the latest changes and news is available at the Advising Hub at http://www.sjsu.edu/advising/.

Consent for Recording of Class and Public Sharing of Instructor Material
University Policy S12-7, http://www.sjsu.edu/senate/docs/S12-7.pdf, requires students to obtain instructor's permission to record the course and the following items to be included in the syllabus:

- "Common courtesy and professional behavior dictate that you notify someone when you are recording him/her. You must obtain the instructor's permission to make audio or video recordings in this class. Such permission allows the recordings to be used for your private, study purposes only. The recordings are the intellectual property of the instructor; you have not been given any rights to reproduce or distribute the material."
    - It is suggested that the greensheet include the instructor's process for granting permission, whether in writing or orally and whether for the whole semester or on a class by class basis.
    - In classes where active participation of students or guests may be on the recording, permission of those students or guests should be obtained as well.
- "Course material developed by the instructor is the intellectual property of the instructor and cannot be shared publicly without his/her approval. You may not publicly share or upload instructor generated material for this course such as exam questions, lecture notes, or homework solutions without instructor consent."

Academic integrity
Your commitment, as a student, to learning is evidenced by your enrollment at San Jose State University. The University Academic Integrity Policy S07-2 at http://www.sjsu.edu/senate/docs/S07-2.pdf requires you to be honest in all your academic course work. Faculty members are required to report all infractions to the office of Student Conduct and Ethical Development. The Student Conduct and Ethical Development website is available at http://www.sjsu.edu/studentconduct/.

Campus Policy in Compliance with the American Disabilities Act
If you need course adaptations or accommodations because of a disability, or if you need to make special arrangements in case the building must be evacuated, please make an appointment with me as soon as possible, or see me during office hours. Presidential Directive 97-03 at http://www.sjsu.edu/president/docs/directives/PD_1997-03.pdf requires that students with disabilities requesting accommodations must register with the Accessible Education Center (AEC) at http://www.sjsu.edu/aec to establish a record of their disability.

Electrical Engineering Department
EE Department Honor Code

The Electrical Engineering Department will enforce the following Honor Code that must be read and accepted by all students.

"I have read the Honor Code and agree with its provisions. My continued enrollment in this course constitutes full acceptance of this code. I will NOT:

- *Take an exam in place of someone else, or have someone take an exam in my place*
- *Give information or receive information from another person during an exam*
- *Use more reference material during an exam than is allowed by the instructor*
- *Obtain a copy of an exam prior to the time it is given*
- *Alter an exam after it has been graded and then return it to the instructor for re-grading*
- *Leave the exam room without returning the exam to the instructor."*

Measures Dealing with Occurrences of Cheating

- *Department policy mandates that the student or students involved in cheating will receive an "F" on that evaluation instrument (paper, exam, project, homework, etc.) and will be reported to the Department and the University.*
- *A student's second offense in any course will result in a Department recommendation of suspension from the University.*

EE118 HONOR CODE
In addition to EE Honor Code, EE118 students understand that professional attitude is necessary to maintain a comfortable academic environment. For examples:

- *I do not just skip the lecture and then ask the instructor to summarize the lecture for me later on. Office hours are for students to have questions, not for the instructor to summarize the lecture for any specific student.*
- *I come to the class on time and leave the class at the end of the lecture.*
- *To minimize possible tension during the exams, I WILL follow the exam rules closely.*
- *I work on the lab assignments and final project by myself.*
- *I understand that long-term learning is my responsibility and so I always keep it up.*
- *I strongly believe that NOT any statement similarly to examples below can be used:*

- *I am working full-time and so do not have enough time for the class.*
- *I have quite many classes this semester and so I do not have enough time for the class.*
- *I just need a passing grade to graduate this semester.*
- *I live far away from the campus and so I can not come to the class often.*
- *etc., etc....*

Relationship to Program Objectives and ABET Program Criteria

Program Objectives	**Course Learning Objectives**	**Level of Support**
(a) An ability to apply knowledge of mathematics, science, and engineering	1-15	Advanced
(b) An ability to design and conduct experiments, as well as to analyze and interpret data	15-16	Advanced
(c) An ability to design a system, component, or process to meet desired needs	1~7	Advanced
(d) An ability to function on multi-disciplinary teams		Moderate
(e) An ability to identify, formulate, and solve engineering problems	1~8	Advanced
(f) An understanding of professional and ethical responsibility		Not supported
(g) An ability to communicate effectively	11,12	Advanced
(h) The broad education necessary to understand the impact of engineering solutions in a global and societal context		Not supported
(i) A recognition of the need for, and an ability to engage in life-long learning	10	Introductory
(j) A knowledge of contemporary issues	10	Introductory
(k) An ability to use the techniques, skills, and modern engineering tools necessary for engineering practice.	8	Advanced
(l) One or more technical specialties that meet the needs of Silicon Valley companies	1~12	Advanced
Program Criteria	**Course Learning Objectives**	**Level of Support**
Knowledge of probability and statistics		Not supported
Knowledge of mathematics through differential and integral calculus, basic sciences, and engineering sciences necessary to analyze and design complex devices	1~7	Advanced
Systems containing hardware and software components	1~7	Advanced

EE118: Digital Logic Circuit Design - Tentative Course Schedule

Subject to change with fair notice as announced by the instructor in class.

Week	Date	Topics	Homework	Laboratory
1	01/24	Introduction		
2	01/29, 31	Boolean Algebra		1
3	02/05	Boolean Algebra	1	2
	02/07	Combinational Circuit /K-Map		
4	02/12, 14	K-Map/Hazards	2	3
5	02/19, 21	Quine-McCluskey Method, Number systems		4
6	02/26, 28	Binary Arithmetic	3	5
7	**03/05**	**EXAM I**		6
	03/07	Multilevel Logic/Comparators	4	
8	03/12, 14	Encoder/Decoder/Multiplexer		7
9	03/19, 21	Flip/Flops	5	8
10	**03/26-30**	**Spring Recess**		
11	04/02	Flip/Flops		9
	04/04	Analysis/Synthesis of Sequential Circuit	6	
12	04/09, 11	Counters/Parallel & Shift Registers		10
13	**04/16, 18**	**Review/EXAM II**	7	11
14	04/23, 25	Data path/Control		12
15	04/30,05/02	Data path/Controller II	8	13
16	05/07, 09	PLD/FPGA Architecture		14
17	05/14	Review for Final		
	05/21	**FINAL EXAM 9:45 to 12:00**		

Lab Schedule (Spring 2018)

EE118

Session Number	Week (Starts on Monday)	Lab Activity (Pre-Lab work is required!)	Remarks
1	01/29/2018	Introduction	Introduction to concepts Purchase Lab kit and manual
2	02/05/2018	Experiment C – Familiarization of TTL ICs (Part I)	Familiarization of TTL ICs
3	02/12/2018	Experiment C – Familiarization of TTL ICs (Part II and III)	Ring Oscillator and Simple function schematic and simulation
4	02/19/2018	Experiment A – Schematic Entry & Simulation of simple & complex functions	Complex function schematic and simulation
5	02/26/2018	Experiment D – Hard-wiring of 2-bit comparator	Building a circuit on a breadboard
6	03/05/2018	Experiment E – Schematic Entry, Simulation and Nexys FPGA Demonstration of the 2-bit Comparators, 7 Segment Display	Repeat the design using FPGA
7	03/12/2018	Experiment F – 4-Bit Comparator and 1-Bit Full Adder: Verilog modeling (hierarchical), simulation, synthesis, and demo on FPGA board	Comparator and Adder
8	03/19/2018	Midterm	Part I: Written Part II: Demo
9	04/02/2018	Experiment G – Flip-flops: Simulation (Part 1)	Sequential
10	04/09/2018	Experiment G – Flip-flops: Hardwiring	Sequential
11	04/16/2018	Experiment H – BCD Counter Design: Hardwiring	Counter
12	04/23/2018	Experiment I – Design & Demo of HEX Counter Using Nexys FPGA Board	Counter
13	04/30/2018	Experiment J – Traffic Light Controller	State Machine
14	05/07/2018	Final Exam	Part I: Written Part II: Demo