On the Design and the Implementation of a Low-power MESI Protocol

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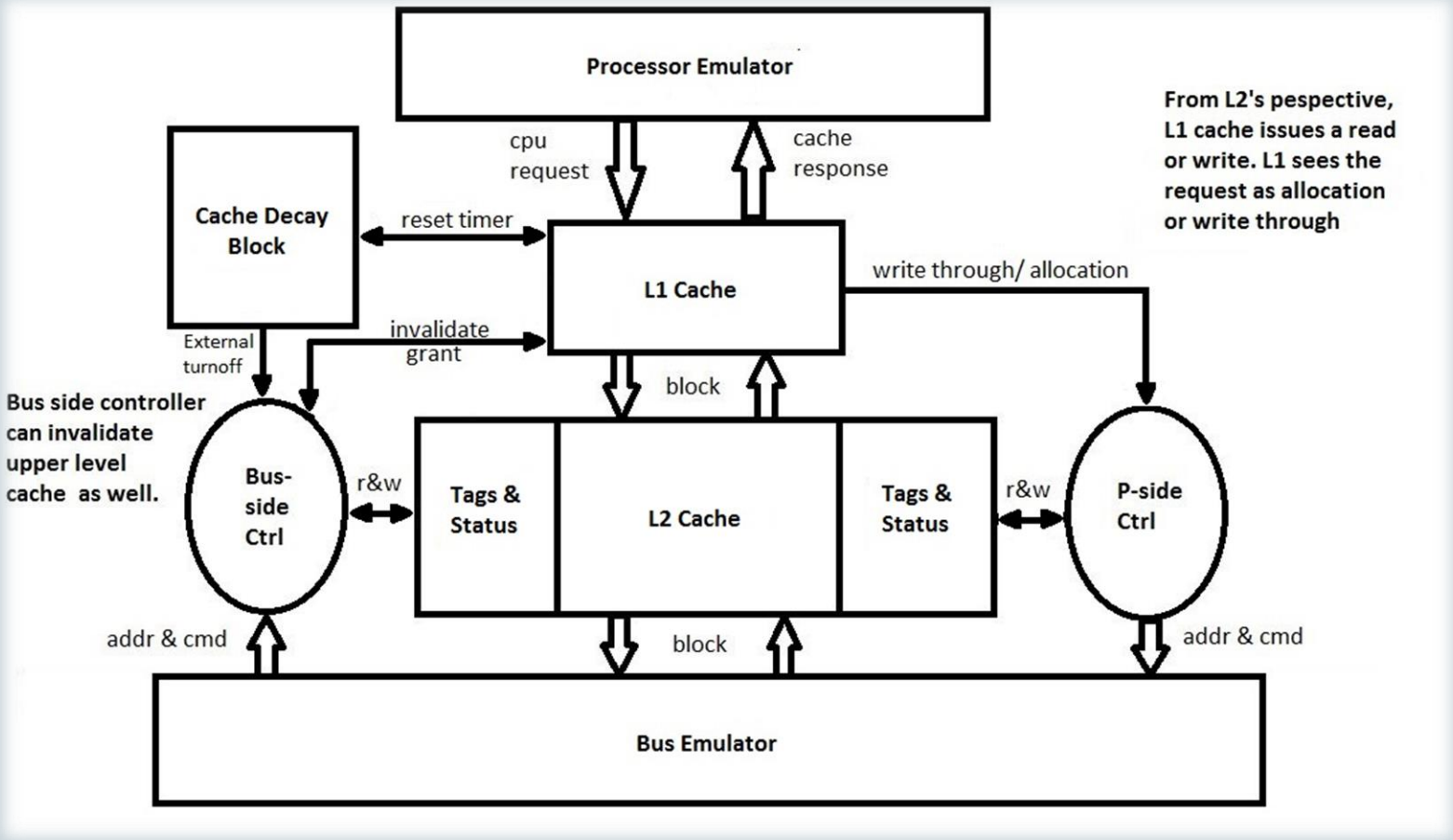
Outline

- Introduction
- Conceptual Design
- Hardware Implementation: Simulation & Synthesis
- Performance Test
- Result Analysis
- Extension
- Conclusion

Introduction

- All mobile devices need low power processors
- All up-to-date processors are multicored
- The objective of this project is to design and implement a low power coherent cache system that reduces the leakage current by using a modified MESI protocol

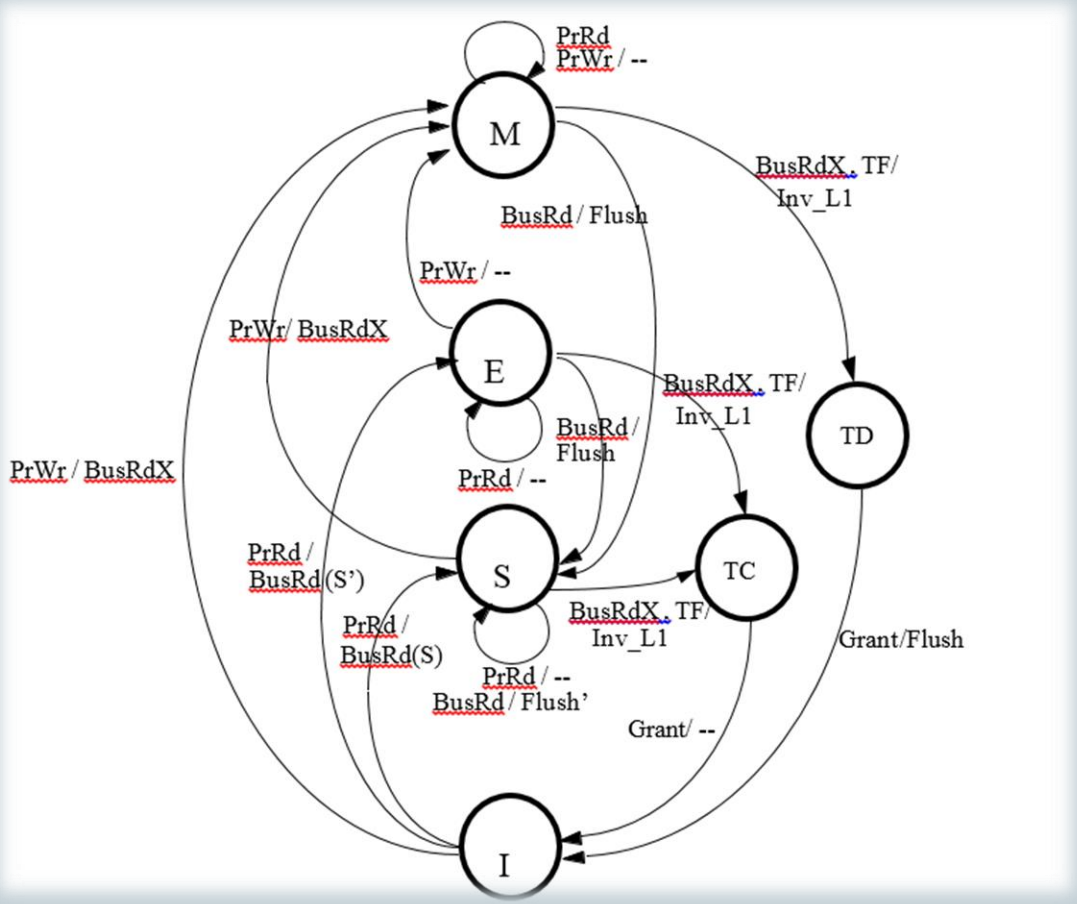
Overview Block Diagram



Hardware Description

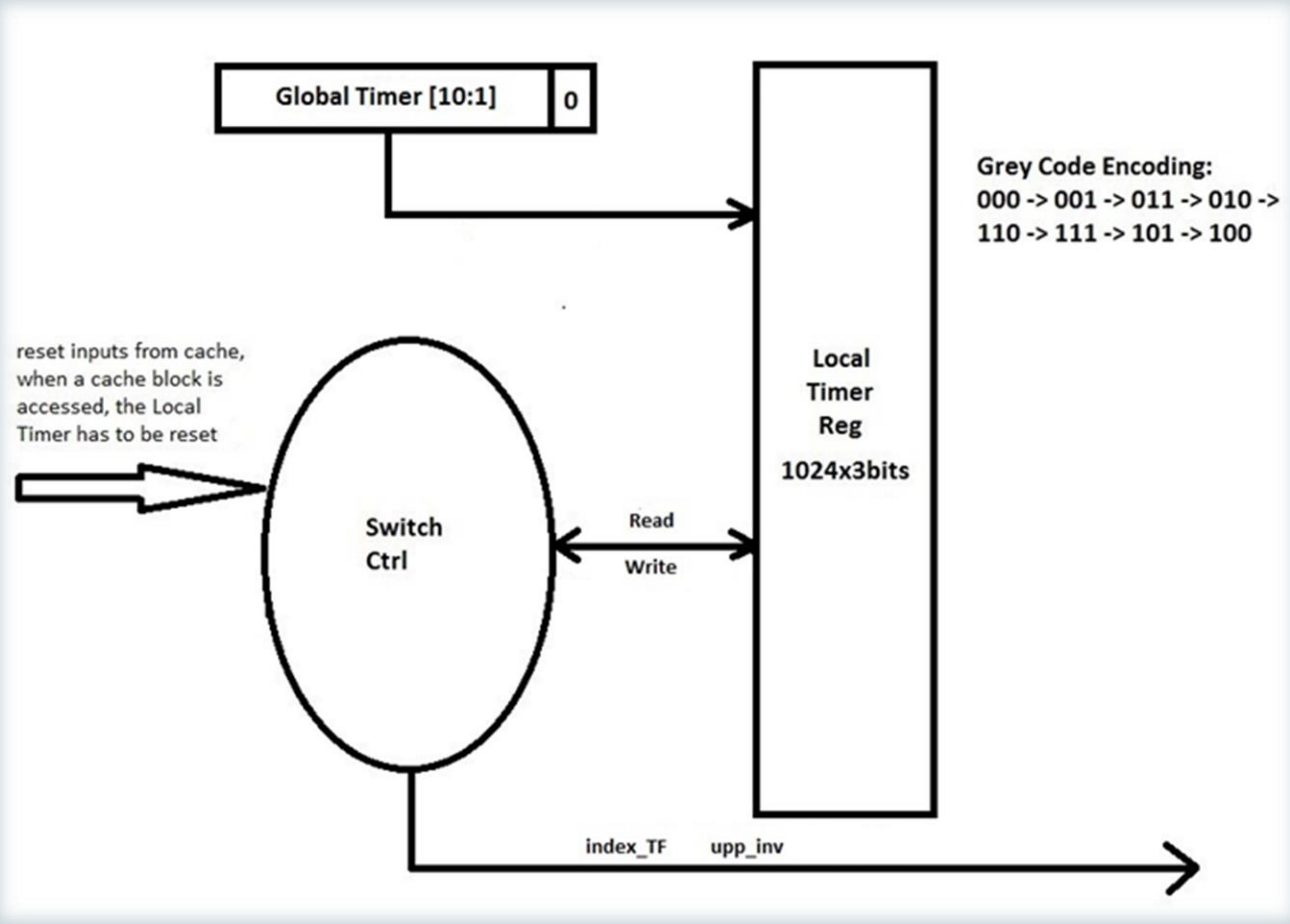
- Two level cache
- Controller with modified coherent cache protocol
- Cache decay block (external turn off)
- Mechanisms to turn off L2 cache block
- Processor Emulator
- Bus Emulator

Modified MESI Protocol



- Transient dirty state
- Transient clean state
- External turn off

Implementation of Cache Decay



Simulation: Functional Test

- Processor write and read test
  - Processor writes and read
  - L1 cache and L2 cache allocation
  - L1 cache and L2 cache evictions
  - L2 cache write back and LRU replacement policy
- Bus read and Bus read exclusive test
  - Bus read & bus read exclusive
  - Flush
- External turn off test
  - External turn off
  - Cache line recover

Synthesis Results

Modified Cache	Timing	Power	Area
L 1 cache	11.23ns	756.99mW	77513.5
L2 cache data path	21.11ns	17.19W	1658165
L2 local controller	3.44ns	2.69mW	308
L2 bus controller	5.01ns	3.28mW	406
Cache decay block	8.12ns	133.06mW	27648.5
Total	n/a	18.09W	1764041

Performance Analysis

- Performance Test
  - Variable settings
  - Random address test cases
  - Locality test cases
- Flexible Variable Setting
  - Randomization feature
  - Private requests rate
  - Shared requests rate
  - Write/read ratio
  - Memory reference address

Random Address Case

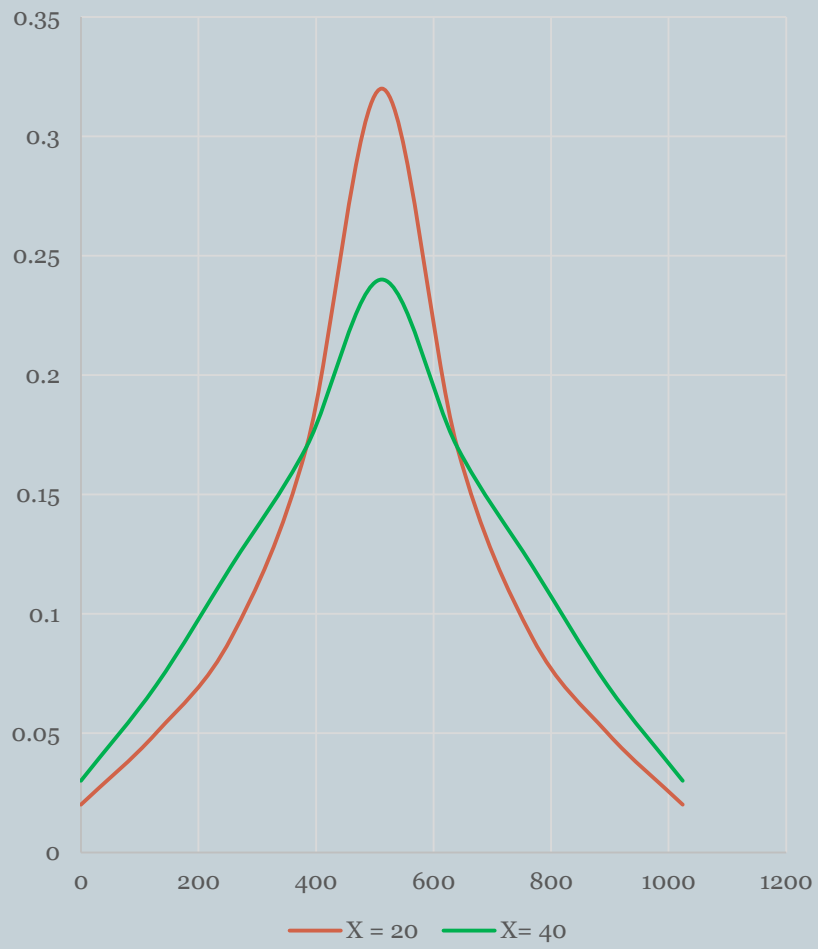
Metrics	Case 1	Case 2
Private requests	8192	16384
Shared requests	973	1912
Execution cycles	45020	90306
Cycles/Private request	5.50	5.51
Cycles/Shared request	46.27	47.23
L2 active cycles	35281558	77253321
Active ratio	76.53%	83.54%
Extra compulsory miss	215(1239)	758(1782)
Extra compulsory miss rate	2.6%	4.6%

$$\text{The Active Ratio} = \frac{\sum (\textit{the Active Time of each cache entry})}{\#\text{ of Cache Entries} * \text{Execution Cycles}}$$

Locality Test Cases

Temporal & Spatial locality

- Variable distance
- Clustering
- Probability of occurrence



Results of Locality Test

Metrics	Case 1	Case 2	Case 3
Distance variable	X = 20	X = 30	X = 40
Private requests	8192	8192	8192
Shared requests	949	947	950
Execution cycles	45198	44932	45017
L2 active cycles	24815487	30058464	31547066
Active ratio	53.62%	65.98%	68.44%
Total compulsory miss	1089	1152	1203
Total compulsory miss rate	13.3%	14.1%	14.7%

Impacts of other important variables

- Shared requests/private requests Ratio

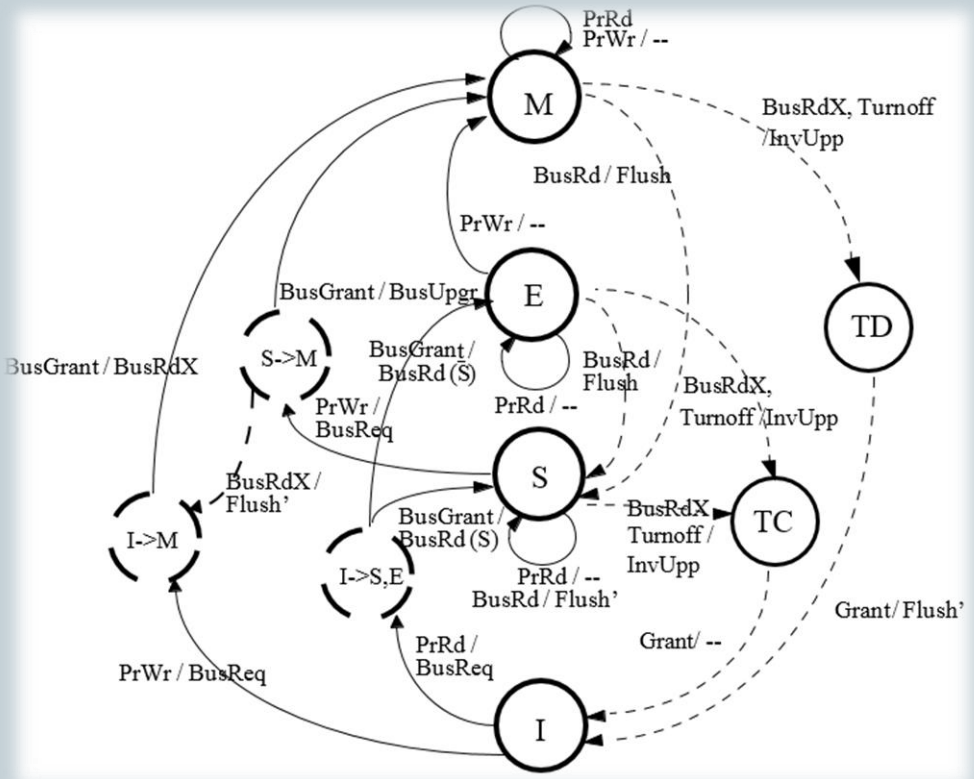
Metrics	Case 1	Case 2	Case 3	Case 4
Shared requests percentage	24.6%	20.3%	15.0%	10.0%
Active ratio	69.9%	74%	75.1%	77.9%
Total compulsory miss rate	10.52%	11.12%	11.02%	10.83%

- Write requests/read requests Ratio

Metrics	Case 1	Case 2	Case 3	Case 4
Write requests percentage	35%	25%	15%	5%
Active ratio	70.67%	73.99%	75.48%	79.33%
Total compulsory miss rate	11.2%	10.49%	10.61%	10.30%

Extension

- Non-atomic State Transition
- Split-transaction Bus
- Tracer Driven Test



Conclusion

- Power saved verses miss rate

Test case	Power Saved	Miss rate (compulsory)
Random Test	16%	+4.6%
Locality Test	20% ~ 30%	+5%

- Cost

  1.6 increases in hardware complexity

Key References

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- [2] M. Monchiero, R. Canal, A. Gonzalez, “Using Coherence Information and Decay Techniques to Optimize L2 Cache Leakage in CMPs,” International Conference on Parallel Processing, ICCP’ 09, pp.1-8, 2009
- [3] S. Kaxiras, Z. Hu, M. Martonosi, “Cache Decay: Exploiting Generational Behavior to Reduce Cache Leakage Power,”Proceedings of 28th Annual International Symposium on Computer architecture. New York, NY, USA: ACM Press, Pages 240-251, 2001

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Thank you !

Questions?