Development of Wear Leveling and Garbage Collection In NAND Flash Memories

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INTRODUCTION

Design and Implementation of a unique algorithm for Wear Leveling and Garbage Collection in the Flash Translation Layer is a necessary requirement for the working of NAND Flash Controller[1].

OVERVIEW

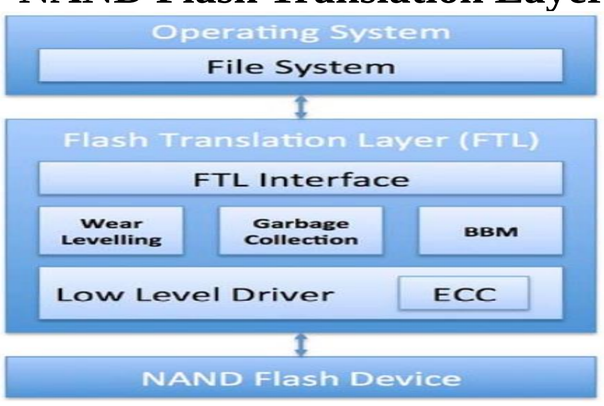
- NAND Flash Memory Organization
- Block IO Tracing mechanism from the kernel, through Blktrace and Perl.
- Test Data: LBA, W/R, no of pages
- Developing an algorithm to carry out Wear Leveling, manage Bad Block and Garbage Collection.

WORKING [2]

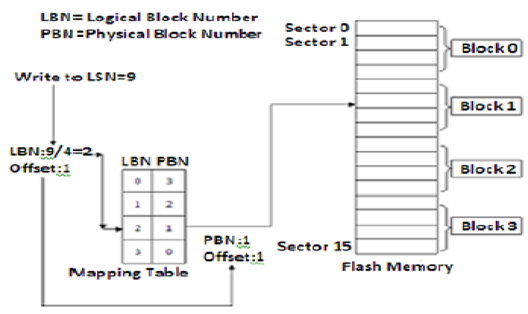
- Maps the logical block address to the physical block address.
- Reads and Writes to the physical memory on the basis of number of pages operated on.
- Sets the status bits in the pages according to Wear leveling.
- Sets a flag to indicate a bad block in the physical memory.
- Erasure of the block occurs with the help of Garbage Collection.

The objective of this work was to design a FSM for the NAND Flash Controller to carry out effective program and erasures on the flash memory.

NAND Flash Translation Layer



ADDRESS TRANSLATION

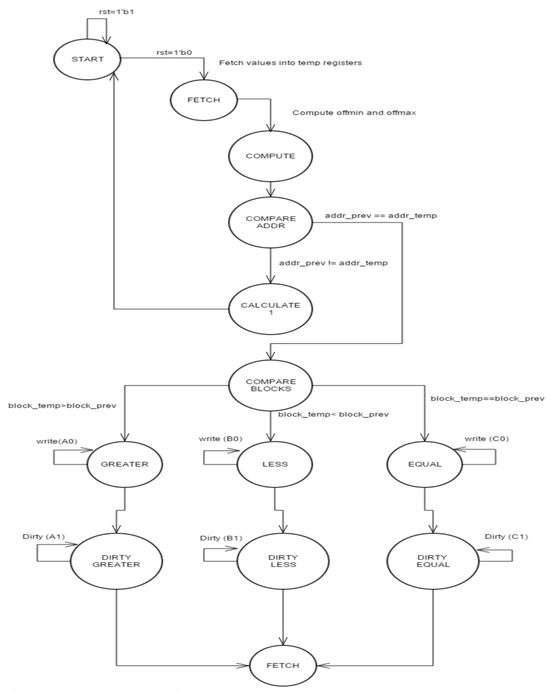


Design Approach

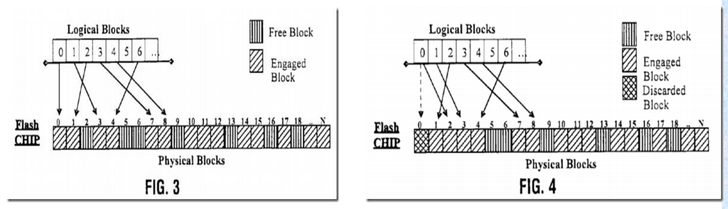
Key Points

- Test Data Generated through the Blktrace
- Built a Finite State Machine for the FTL
- Write/ Read to a Page and Block Erasure

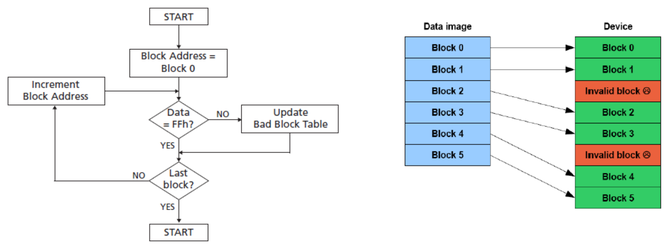
State Diagram for Wear Leveling [1]



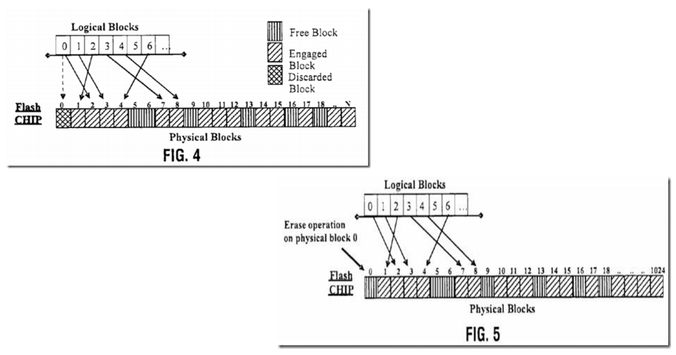
Wear Leveling Flow



Bad Block Management [3]

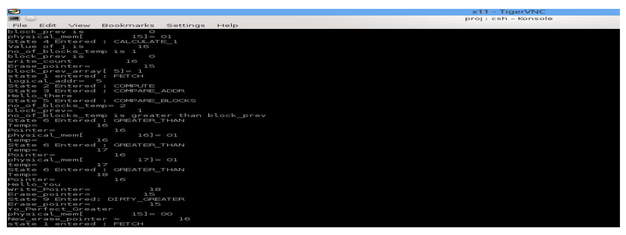


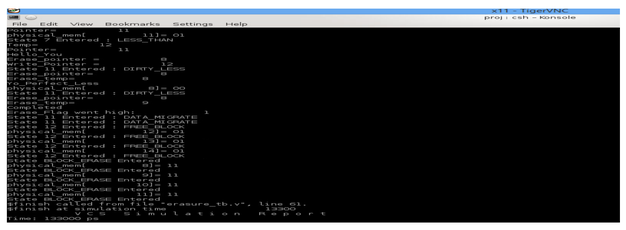
Garbage Collection [3]



Results

Test data extracted using Blktrace utility and PERL. Basically used 3 different fields to carry out Wear Leveling and Garbage Collection.

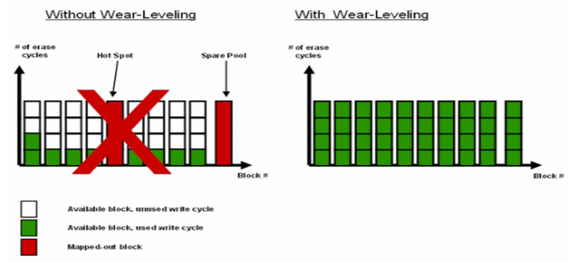




Understanding the output

EMPTY/ERASED : 2'b11 USED: 2'b01 STALE: 2'b00

BBM and GC promises



Challenges and Solutions

Design 1 Challenges: Only worked on Write/Erase Cycles. Couldn't implement actual WL, GC and BBM.

Design 2: Implemented an algorithm for the entire Flash Translation Layer.

Advantages:

Effectively Writes/Erases blocks

Implements WL, GC and BBM

Design 2 Challenges: Maintain List of free blocks

Solutions: Reserved Block Method

Conclusions

We have presented a finite state machine model of the modules that reside in the Flash Translation Layer. I thorough demonstration of distribution of the Program/ Erase Cycles was shown in this project work. The algorithm ensured that most of the physical flash memory was always available for read write operations and never wore out. No blocks reached its maximum erase and write counts. The algorithm displayed the performance of the erasures occurring on the blocks by the Bad block management and Garbage Collector.

Key References

[1] Micron Technology, Inc., "Tn-2961 Wear Leveling". [Online] Available: https://www.micron.com/~/media/documents/products/technical-note/nand-flash/tn2961_wear_leveling_in_nand.pdf

[2] Rino Micheloni, Luca Crippa, Alessia Marelli ,"Inside NAND Flash Memories" , Springer

[3] Stmicroelectronics, "Bad Block Management and Garbage Collection". [Online] Available:

http://www.eetasia.com/ARTICLES/2004NOV/A/2004NOV29_MEM_AN06.PDF?SOURCES=DOWNLOAD

Acknowledgments

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For further information

Please contact *surajdk8@gmail.com*. Verilog HDL code, PERL Script, simulation files and research material are available upon request.