Implementation of Verification IP for ACE Cache Coherency Protocol

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INTRODUCTION

- ACE cache coherency protocol is a complex protocol to verify.
- Verification IP are hard for customers to understand.
- Goal of the project is to reduce effective time involved in verification and achieve early time to market.
- Enable plug and play feature to make the VIP importable to any cache coherency protocol system.
- Project increases scalability and reusability by adopting Universal Verification Methodology.

FEATURES

Reusable Components

- ace master agent
  - Has a driver, sequencer, monitor and a predictor.
  - Can be made active or passive through agent configuration class.
- ace master driver
  - Converts packets into interface signals.
  - Has a handle for virtual interface(vif).
- ace master monitor
  - Reads pin level signals and transfers into packets.
  - Has an analysis port which transfers packet to the scoreboard.
- Each components are connected together through TLM ports.
- TLM ports enhances reusability and portability by making components independent of each other.
- Predictor is used for unit level verification when single master is used.

FEATURES

Reconfigurable IP

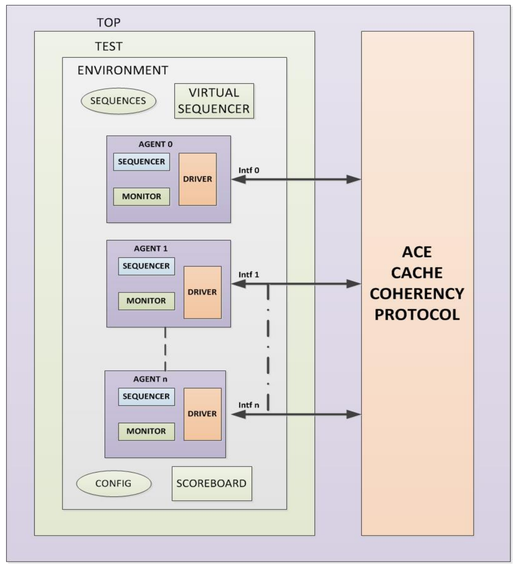
- Reconfiguration is done using system configuration class and agent configuration class.
- System configuration
  - Configures number of masters.
  - Configures port ID for initiating master and snoop master.
- Agent configuration
  - Configures active/passive agent.
  - Configures interface for each masters.
- Configuration objects are set from the test case.
- Gives more flexibility for the user to overwrite and configure from top level.
- User configuration file is used to provide user defined values.

FEATURES

- Plug and Play Module
  - Instantiate DUT and the interface in the top.sv file
  - VIP test cases will take care of connecting the interface to the environment.
  - This is done using powerful feature set and get configuration database of UVM.
- Supports fully associative cache.
  - Cache line size and number of cache lines are user configurable.
  - Cache line is dynamically allocated and deleted.
  - Improves runtime and simulator performance.
- Comprehensive protocol checks is done using System Verilog Assertions (SVA).
  - Supports both concurrent and immediate assertions.

SYSTEM ARCHITECTURE

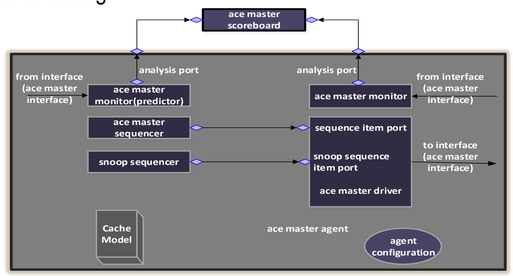
- Supports 128 masters.
- Has a virtual sequencer to route packets between 2 different agents.
- System configuration class is used for environment configuration.
- Sequences randomizes the sequence item and transmits to the sequencer.
- Driver receives the packet from the sequencer and drives it to the interface.
- System level scoreboard is used to check transaction across different masters.



Block Diagram of the Cache Coherency VIP

BUS FUNCTIONAL MODULE

- Driver has 2 ports – one for sending coherent transactions and another for snoop transactions.
- Supports both AXI and ACE cache coherency Interface.
- Agents can be active or passive.
- Cache model is associated with each agent.
- Scoreboard is used for both unit level testing and block level testing.



Block Diagram of the Bus Functional Module

CONNECTING WITH USER ENVIRONMENT

- Configure the parameters in user configuration file.
  - INITIATING_MASTER ,SNOOP_MASTER.
  - NUMBER_OF_CACHE LINES.
  - BURST_LENGTH , BURST SIZE
  - NUM_OF_MASTERS
- Set the interface from the top module. VIP configures each interface to its respective agents.
- Use option +define+BUS_TYPE_ACE to run ACE specific transaction.
- Run the test using Make test="test_name" command.
  - eg . Make test=read_unique_test.

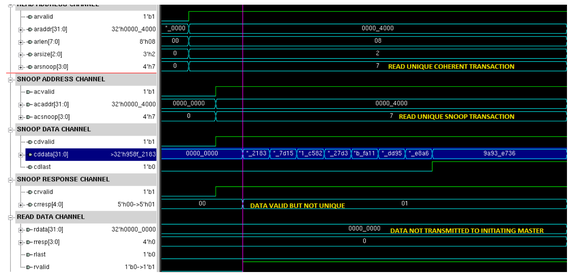
RESULTS AND OBSERVATIONS

- STEP1: Master initiates coherent transaction asking for unique data [3].
- STEP2: Interconnect receives coherent transaction and initiates snoop transaction .
- STEP3: Snoop master receives snoop request and generates unique data if available
- STEP4: Master 2 updates the status in response channel
- STEP5: Interconnect seeing the unique status provides data to the initiating master.

Read Unique transaction

RESULTS AND OBSERVATIONS

- Snoop master gives a shared status to the Interconnect.
- Interconnect doesn't provides data to the Initiating master.



Read Unique transaction failure case

CONCLUSION

- Supports up to 128 masters.
- Supports both unit level and block level testing.
- Cache coherency is demonstrated and verified using block level testing.
- Supports all kinds of coherent and snoop transactions.
- Designer can easily modify the VIP according to his specification needs.
- Protocol checks are done using SystemVerilog Assertions(SVA).

FUTURE WORK

- To support DVM and barrier Transactions.
- To support snoop filter.
- To support all kinds of cache.
- To implement a cache controller.

REFERENCES

- [1] ARM. AMBA AXI and ACE Protocol Specification, Feb. 2013. Version ARM IHI0022E.
- [2] A. Stevens. Introduction to AMBA 4 ACE. ARM whitepaper, June 2011.
- [3] C. Thompson. Verifying Cache Coherency Protocols with Verification IP. Synopsys,Oct. 2012.

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