Modeling a new technique of phase detection for clock and data recovery applications

Ms. Deepika Vyas, Dr. Shahab Ardalan

Department of Electrical Engineering, San Jose State University, San Jose, California 95192

Introduction

Phase detectors are an integral part of frequency synthesis and phase detection circuits at the receiver end of any high speed transmission system.

Phase detector topologies;

- Linear phase detector provides both sign and magnitude information of phase difference between clock and data with low timing jitter[1].
- Binary Phase detectors provide only sign information regarding the phase difference with lower locking time[1].
- Advance phase detector combines linear phase detector with the binary phase detector to achieve fast locking and low timing jitter[2].
- Linear phase detector operates when the phase difference is between the region - π/4 to π/4.
- Binary phase detector operates when the phase difference is between region - π to -π/4 and from π/4 to π.
- To achieve this operation an Improved binary phase detector is developed which produces zero output when the phase difference is between the region - π/4 to π/4 and operates like a bang-bang phase detector when the phase difference is between region - π to -π/4 and from π/4 to π.

Three different phase detector topologies were implemented in the PLL based CDR architecture using MATLAB/Simulink, Verilog-a and 45nm CMOS technology simulators with successful improvements in performance parameters of Advanced phase detector at 2GHz clock frequency.

Modeling

The simulation models are designed based on the following equations

$$F_{vco} = F_o + K_{vco}.V_c \quad (1)$$

where F_{vco} is a control voltage dependant function which aims to capture the phase changes in the input. K_{vco} is the gain of the voltage controlled oscillator (VCO). F_o is the center frequency of the VCO. C is the loop filter capacitance.

$$W_n = \sqrt{\frac{I_{cp} * K_{vco}}{2\pi C}} \quad (2)$$

I_{cp} is the charge pump current which defines the stability factor and natural frequency (Bandwidth) of the clock and data recovery loop.

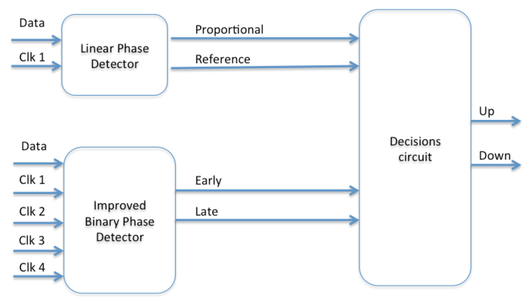
$$z = \frac{R}{2}\sqrt{\frac{I_{cp} * K_{vco} * C}{2p}} \quad (3)$$

Design Approach

Key Points

- Low timing jitter
- Fast locking time
- High speed and low power consumption

Advanced Phase Detector Block Diagram



Phase detector S-curve Comparison

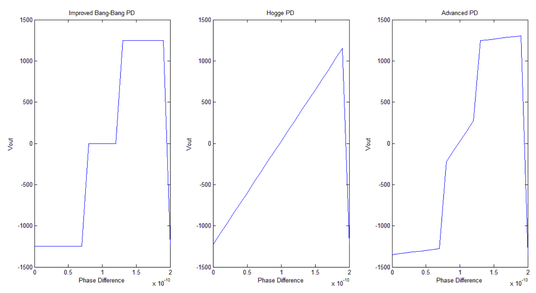
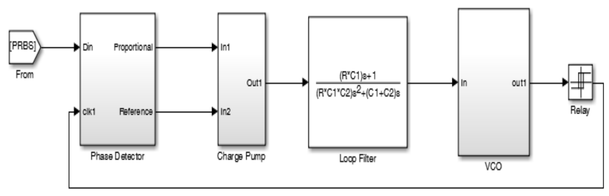


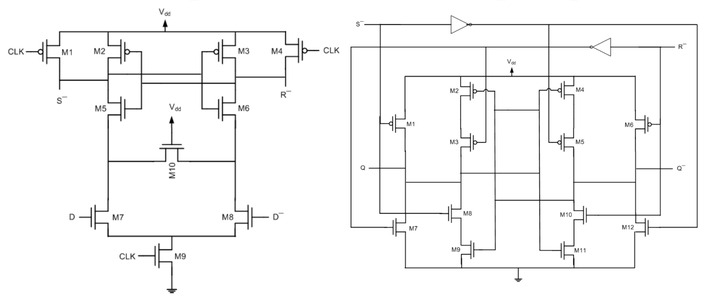
Figure depicts the transfer characteristics of Improved bang-bang, Linear and Advanced phase detectors respectively.

System Diagram for CDR



The system diagram for a clock and data recovery circuit [3]. Major blocks of the design are Phase detector, Charge pump, Low pass filter and VCO.

Circuit Implementation For D Flip-Flop

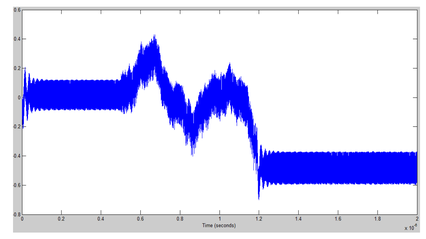


Sense Amplifier SR Latch

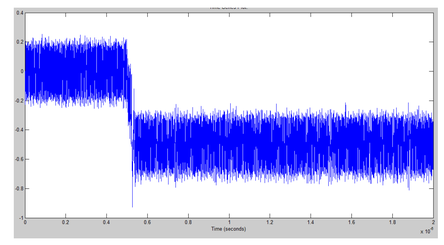
Sense Amplifier based flip flop design[4] was built using 45nm technology in Cadence. Full swing outputs can be generated for high speed low swing inputs with low power consumption.

Results

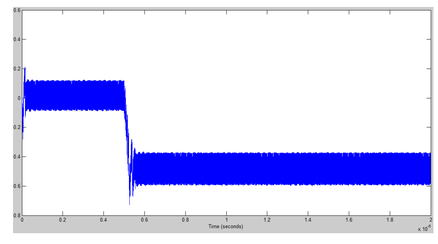
Control voltage for linear, binary and advanced phase detectors



Response of control voltage of Hogge PD for frequency shift of 500 MHz-shows **less jitter** and higher lock time in comparison to Binary PD.



Response of control voltage of Alexander PD for frequency shift of 500 MHz-shows **less lock time** and higher jitter in comparison to Linear PD.



Response of control voltage of Advanced PD for frequency shift of 500 MHz-shows **reduction in both lock time and timing jitter.**

Parameter	Binary PD	Linear PD	Advanced PD
Lock Time	100ns	500ns	**100ns**
Timing Jitter	65ps	25ps	**25ps**

Conclusions

A new technique of phase detection was presented that displays performance improvements with respect to the jitter and lock time in the clock and data recovery circuit. The D flip flop utilized for implementing the phase detector topologies was designed using an improved sense amplifier based flip-flop circuit in 45nm CMOS technology. This topology enables high speed of operation ranging in GHz. Low Jitter can be achieved by utilizing the characteristics of a Linear Phase detector and lower lock time can be achieved by implementing the characteristics of a Binary phase detector.

Key References

[1] B.Razavi, “Design of Integrated Circuits for Optical Communications,” McGraw-Hill, New York, 2003.

[2] J.Li, and F.Yuan,”A Hybrid Phase Detector for reduced Lock Time and Timing Jitter of Phase-Locked Loops,”Analog Integrated Circuits and Signal Processing, Vol.56, No.3, pp.233-240,Sep.2008.

[3] Hsieh, Ming-ta, and G. Sobelman. "Architectures for multi-gigabit wire-linked clock and data recovery." Circuits and Systems Magazine, IEEE 8.4 (2008): 45-57.

[4] Nikolic, Borivoje, et al. "Improved sense-amplifier-based flip-flop: Design and measurements." Solid-State Circuits, IEEE Journal of 35.6 (2000): 876-884.

Acknowledgments

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For further information

Please contact *deepika.vyas@sjsu.edu.* MATLAB code, Verilog-a code and circuit simulation files are available upon request.