A FPGA-Based Real-Time Stereo Vision System with Improved SGM Path Cost Propagation Method

Chia-Pin Tseng, Boyang Wang, Chang Choo

Department of Electrical Engineering, San Jose State university, San Jose, California 95192.

Introduction

In this paper, we used Xilinx Spartan-6 FPGA and VMOD-CAM to achieve the real-time SGM based stereo vision system. This implementation utilized 54,576 slices registers, 2,288 LUTs, and the maximum pixel clock frequency up to 71 MHz. The performance is equivalent to HD stereo source video sequence at the rate of 40 frames per second, generating 32 pixel range disparity maps. We also introduced a novel branch SGM method to provide robust noise reduction ability to SGM method. The branch SGM method reduced 10%~25% average error under absolute difference (AD) metrics.

Background

In this paper, We chose Semi-Global Matching (SGM) algorithm as our base algorithm. It produced very good outcome considering the simplicity of the algorithm. In addition, by the smoothness constraint mechanism, it avoided the aperture problem and provided ability to tolerate objects of various sizes and performed good disparity map.

However, SGM could only obtain the information from the particular paths. Some important features information might be ignored due to the sparse sampling. Therefore, we introduced a novel branch path propagation method to let each path can actively share and search the features information.

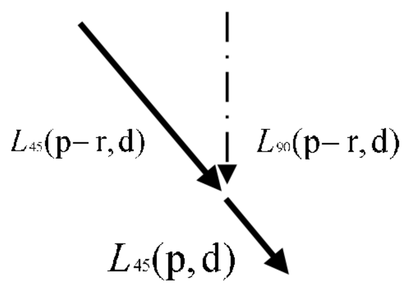
Architecture and Algorithm

We modified SGM equation, so that every path had ability to share neighboring paths information.

Architecture and Algorithm

These two equation on the left was almost identical to SGM equation, but we added a middle variable Lr'(p,d). There was an additional equation working as a bridge between Lr'(p,d) and Lr(p,d).

Every path tried to create a branch toward the highest cost. For example, if L45(p-r,d) is smaller than L90(p-r,d), then, according to the equation, L45(p,d) will be the sum of αL45(p-r,d) and (1-α)L90(p-r,d).



We named this algorithm as branch SGM. Branch SGM algorithm reduced output noise by actively gathering the feature information .

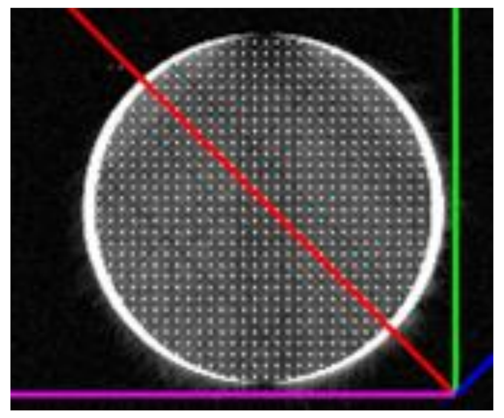


Figure 1: Original SGM

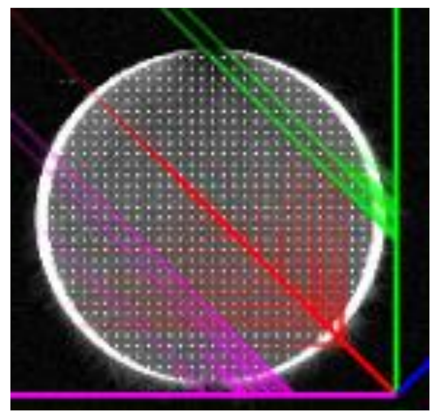


Figure 2 : Branch SGM

Since every path had more information about features, branch SGM was able to provide higher SNR of S(p,d) comparing to the SGM method. The S(p,d) plot for SGM and branch SGM were shown as below. Our method provided lower noise and was able to tell the "black tunnel"

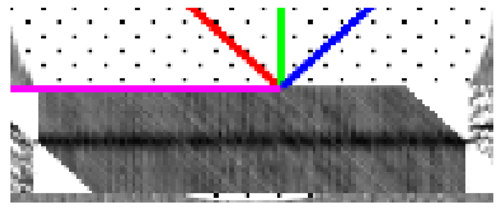


Figure 3 : S(p,d) of SGM

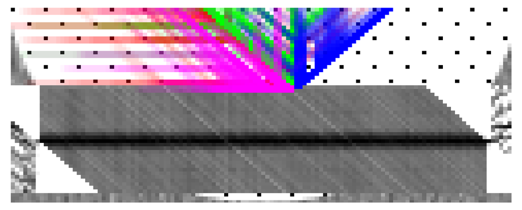


Figure 4 : S(p,d) of branch SGM

The traditional way to handle high noise disparity pair was to raise the penalty parameters P1 and P2. However, high P1 and P2 led blurred disparity edge. Our method allowed stereo matching engine to resist the input image noise and remain low penalty parameters.

Design and Implementation

We implemented the branch SGM algorithm on Spartan6 FPGA. The branch SGM hardware structure is illustrated as below

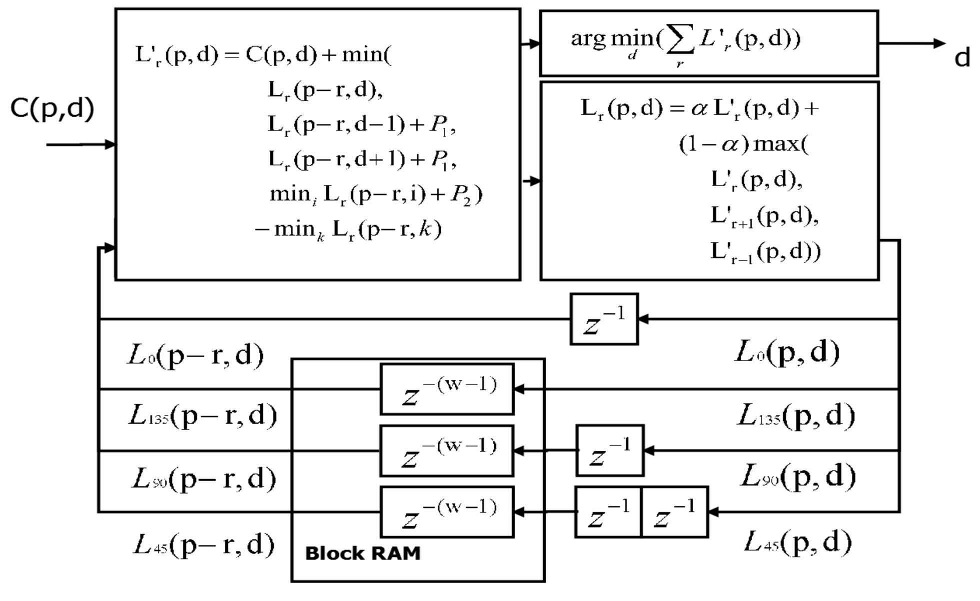


Figure 5: Branch SGM diagram

The path direction was produced by long shift register. To reduce the logic resources utilization we did not utilize real shift register, instead, we used block RAM to simulate the behavior of shift register.

Figure 6: stereo matching system

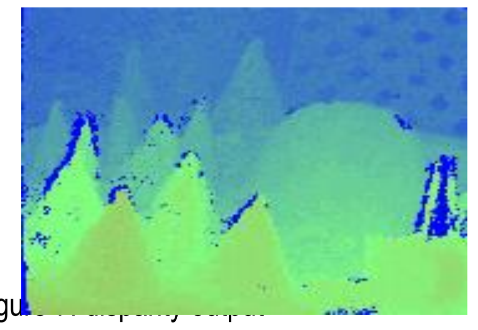


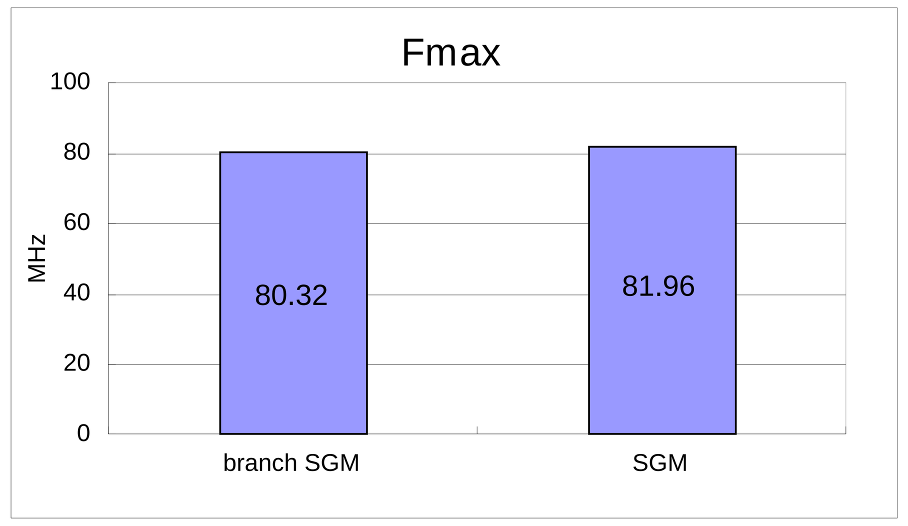
Figure 7: disparity output

Discussion and Analysis

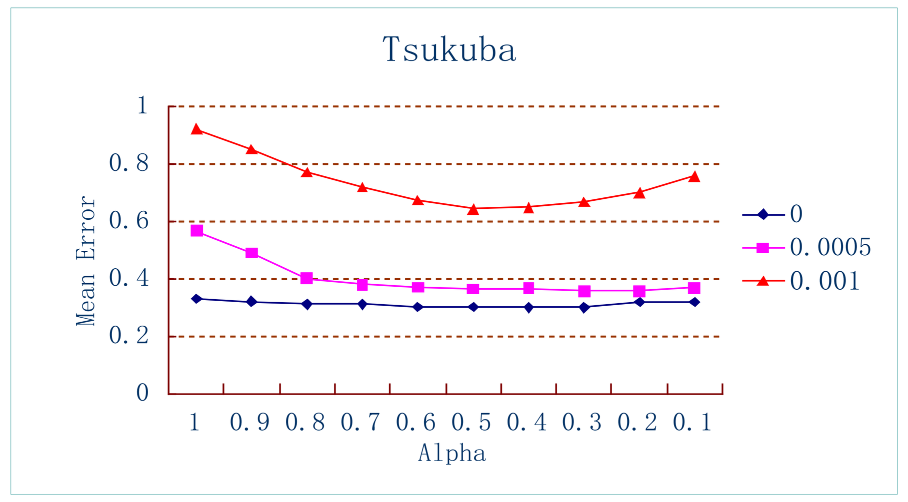
	register	LUTs	Block RAM (18Kb)
SGM	6519	10625	130
Branch SGM	6907	11748	130

table 1: Our SGM and branch SGM IP core resources utilization

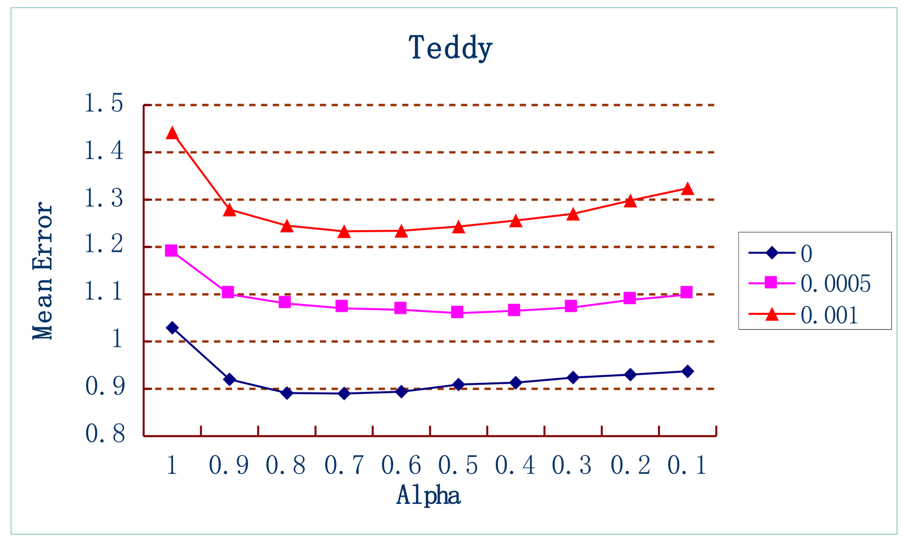
Our branch SGM utilized 6% more slices register and 10% more LUTs.



Plot 1: Our SGM and branch SGM IP core Fmax



Plot 2: Branch SGM performance under different noise level



Plot 2: Branch SGM performance under different α and noise level

Usually when noise level goes higher branch SGM can provide better improvement

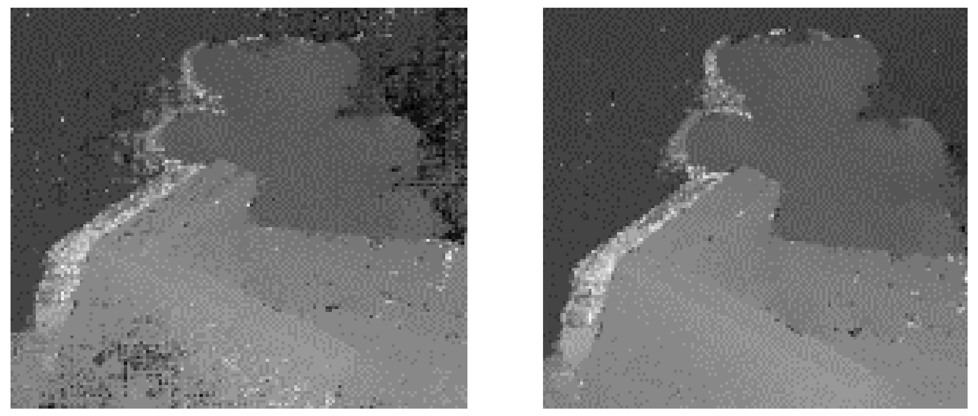


Figure 8: SGM result and branch SGM result(Variance = 0.0005, α = 0.6)