Implementation of Verification IP for AMBA AXI Communication Protocol

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Introduction

- AMBA AXI [1] is a complex protocol to verify.
- Verification IP are hard for customers to understand.
- Goal of the project is to reduce the effective time involved in verification and early time to market.
- Enable Plug and Play feature to make the VIP importable to any AXI protocol system.
- Project increases scalability and reusability by adopting UVM.

Features

Reusable Components

- ace master agent
  - Has a driver, sequencer, monitor and a predictor.
  - Can be made active or passive through agent configuration class.
- ace master driver
  - Converts packets into interface signals.
  - Has a handle for virtual interface (vif).
- ace master monitor
  - Reads pin level signals and transfers into packets.
  - Has an analysis port which transfers packet to the scoreboard.

Features

Reconfigurable IP

- IP is reconfigurable using system configuration class and agent configuration class.
- System Configuration
  - Configures number of masters.
  - Configures port ID for initiating master.
- Agent Configuration
  - Configures active/passive agent.
  - Configures interface for each master.

Plug and Play Module

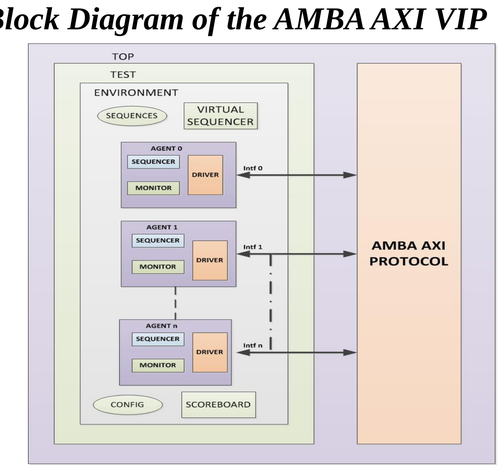
- Instantiate the DUT and interface in the top.sv file.
- VIP test cases will take care of connecting the interface to the environment.
- This is done using powerful feature set and get configuration database [2] of UVM.

System Architecture

Key Points

- Supports 128 masters.
- Has a virtual sequencer to route packets between 2 different agents.
- System configuration class is used for environment configuration.
- Sequences randomizes the sequence item and transmits to the sequencer.
- Driver receives the packet from the sequencer and drives it to the interface.
- System level scoreboard is used to check transaction across different masters.

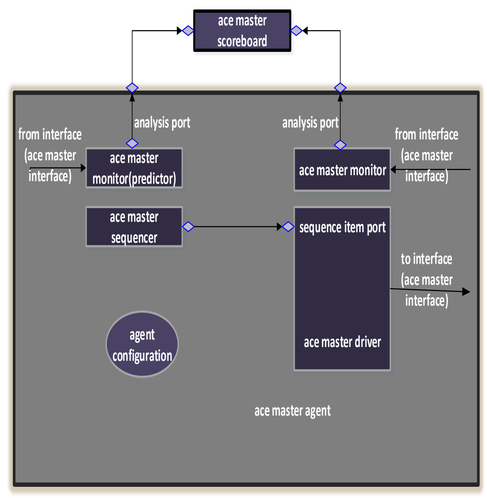
Block Diagram of the AMBA AXI VIP



Bus Functional Module

- Driver has in built ports for transmitting write and read transaction.
- Supports both AXI and ACE Interface.
- Agents can be active or passive.
- Scoreboard is used for both unit level testing and block level testing.

Block Diagram of the Bus Functional Module

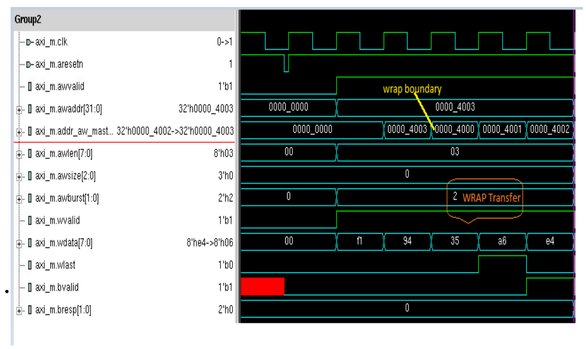


Connecting With User Environment

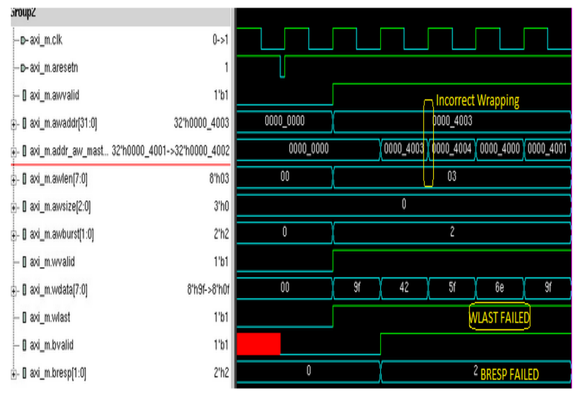
- Configure the parameters in user configuration file.
  - ➢NUM_OF_MASTERS
  - ➢ INITIATING_MASTER
- Set the interface from the top module. VIP configures each interface to its respective agents.
- Make test=“test_name” command is used to run tests.

Results

Write Transaction of Burst Length 4 (Test Passed)



Write Transaction of Burst Length 4 (Test Failed)



Conclusions

- Supports up to 128 masters.
- Supports both unit level and block level testing.
- Supports all kinds of read and write transactions.
- Designer can easily modify the VIP according to his specification needs.
- Protocol checks are done using SystemVerilog Assertions(SVA) [3].

Key References

[1] ARM AMBA Protocol Specification (2010)[Online]. Available: http://www.infocenter.arm.com

[2] UVM Cookbook., Verification Academy., Mentor Graphics., Fremont, CA

[3] Vassilios Gerousis, IEEE-1800-2009, SystemVerilog Language Reference Manual, 2009

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For further information

Please contact vivek.muralidharan@sjsu.edu for additional details and soft copies of the source code.