FPGA Based Real Time Optical Flow Computation

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Introduction

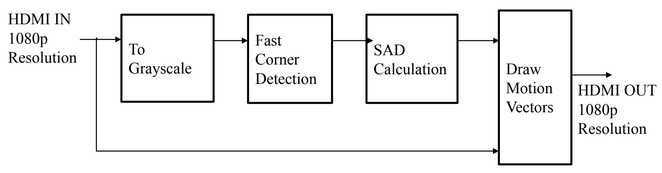
One of the key tasks in driverless car is computing optical flow of the objects around the car in real time. The goal of this project is to implement FPGA based real time motion detection. Project is divided into three main domains:

1. **FAST** (*Features from Accelerated Segment Test*)
2. **SAD** (*Sum of Absolute Difference*) based Block Matching Algorithm
3. **Integrating** FAST and block matching algorithm on FPGA

The system was implemented on Xilinx Zynq zc702 with a FMC imageon card on it. Hardware runs at frequency of 150 MHz and utilizes about 39% LUTs. The resulting system can run for a real time video stream with HD resolution of 1980x1080at 60fps.

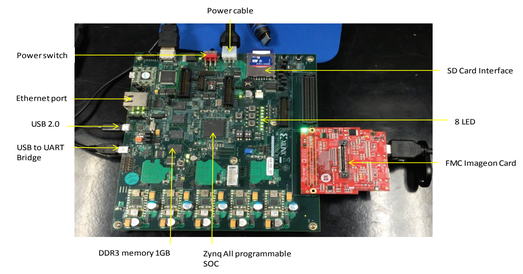
We have implemented the integration of FAST and SAD based block matching algorithm on Xilinx Zynq zc702 FPGA.

Design Approach



- HDMI input is interfaced with the Zynq zc702 through FMC Imageon card. The input resolution is 1980x1080 with frame rate of 60fps.
- In FAST algorithm, a reference pixel considered with intensity Ip. A Bresenham circle is considered around the reference pixel, by presetting a particular threshold value, each pixel on the Bresenham circle is compared with the threshold value for determining if the reference pixel is the corner point.
- SAD/Correlation based pixel matching finds the motion vector of the image by comparing the pixel to the corresponding pixel in the neighboring image. This is achieved by finding sum of absolute differences between each pixel and corresponding neighboring pixel.
- SAD based block matching algorithm is performed only on the feature points found from FAST algorithm.
- The motion vectors are observed through arrows indicating the motion on HD screen.

Hardware Description



Zynq ZC702 family is based on all programmable SOC architecture . It consists of :
Dual- core ARM Cortex A-9 Based Application Processor, 256 KB on-chip RAM, 16-bit or 32-bit interfaces to DDR3, DDR3L, DDR2, or LPDDR2 memories, 1GB of address space using single rank of 8-, 16-, or 32-bit-wide memories

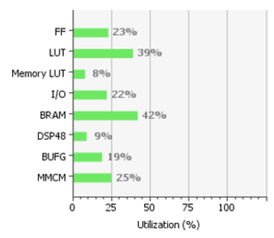
Vivado HLS 2014.4

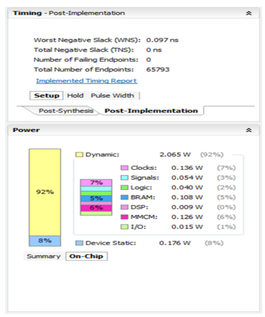
Vivado HLS accelerates IP creation by enabling C, C++ and System C specifications to be directly targeted to Xilinx All Programmable devices without need to manually create the RTL.

Results

The above figure displays the motion vectors for a real time video stream captured through webcam and fed through HDMI IN port of the FMC Card. Unlike the motion estimation obtained through SAD based block matching algorithm, the motion vectors are computed and displayed only after corners are detected and if there is any motion. Here only the hand is moved and hence motion vectors are displayed only for hand and at the tip of fingers.

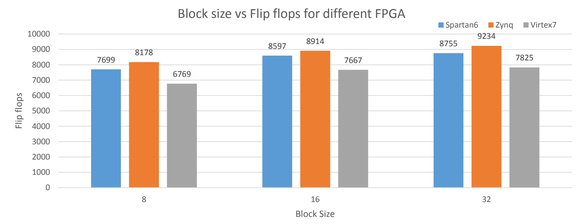
Utilization

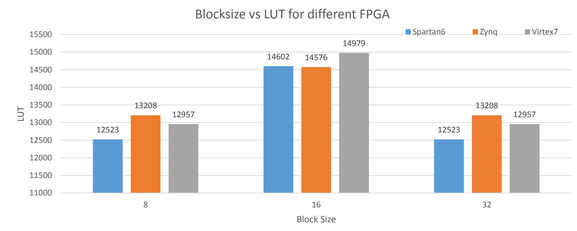


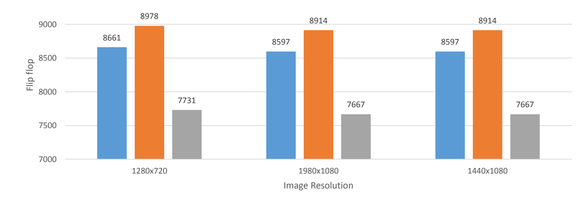


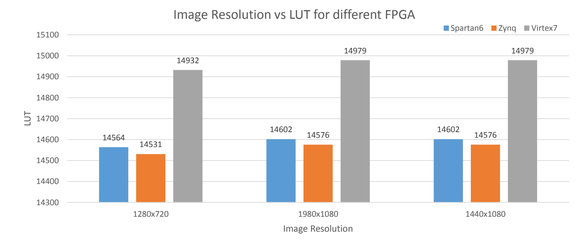
Analysis

- From utilization report, it is observed that design utilizes about 39% of available LUTs and 22% of available flip flops. And Memory utilization is only about 8%.
- Timing analysis shows worst negative slack of 0.097ns. From Power analysis it is observed that total dynamic power is 2.06W and static power 0.176W.
- Following charts display Number of LUTs and Flip flops utilized for different FPGAs and for different image resolution.









Conclusion

Comparison of real time optical flow computation done by SAD based block matching algorithm method and FAST + SAD based block matching algorithm method, it is seen that the computation done by FAST + SAD based block matching algorithm is not only faster but it also removes unwanted noise. Implementation of optical flow by SAD based algorithm, determined motion vectors for each and every pixel including unwanted noise. FAST corner detection algorithm helped to remove the unwanted noise.

Key References

[1] Zynq-7000 EPP ZC702 Base Targeted Reference Design User Guide
www.xilinx.com/support/documentation/boards_and_kits/ug925-zynq-zc702-base-trd.pdf

[2] Xilinx Vivado HLS:
www.xilinx.com/support/documentation/application_notes/xapp1167.pdf

[3] E. Rosten and T. Drummond, "Machine learning for high speed corner detection," in 9th European Conference on Computer Vision, 2004.

[4]M. Kraft, A. Schmidt, and A. J. Kasinski, "High-speed image feature detection using fpga implementation of fast algorithm," 2001.

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For further information

Please contact akhule7@gmail.com or *minjalppatel@gmail.com*. Opencv code, simulation files and RTL codes are available upon request.