FPGA Based Stereo Vision System design

Disparity Mapping

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Introduction

- The concept is inspired by human eye and brain coordination system which enables us to get the idea of three dimensional views in surrounding [1].

- The system calculates disparity of the object in the image by comparing frames received by two cameras at the same instant but displaced on horizontal plane.

Hardware for Disparity Mapping System:

- Altera DE1 platform has been used in the project. The Cyclone II FPGA provides high performance logic, higher capacity, higher performance, and high amount of resources than earlier designs.

- It has on board 18,752 logic elements, 4 PLL, 52 M4K RAM blocks, 26 embedded multiplier, SD card socket, RS232 and VGA out connector.

Applications:

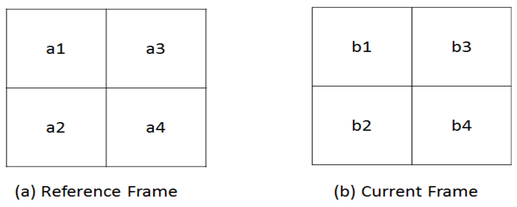
- Object detection/tracking in driverless cars.
- Factory automation to ensure product quality.
- Human – computer interactive systems.

Algorithm

Sum of Absolute differences (**SAD**) algorithm used for measuring the similarity between image blocks

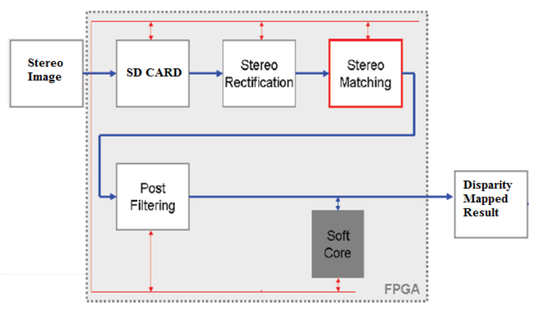
$$\sum_{(i,j)\in W} |I_1(i,j) - I_2(x+i, y+j)|$$

It works by taking the absolute difference between each pixel in the original block and the corresponding pixel in the block being used for comparison. These differences are summed to create a simple metric of block similarity [2].



Design Approach

Block Diagram of the System



System Implementation

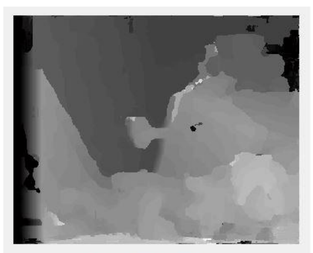
The implementation strategy for the project included systematic phase wise approach which involved development and testing on different platforms for all the stages from prototyping to the design of final system.

The sequential progress could be classified in terms of following two broad categories [3]:

- Prototype to Development
- Algorithm Expansion

Left Stereo Image

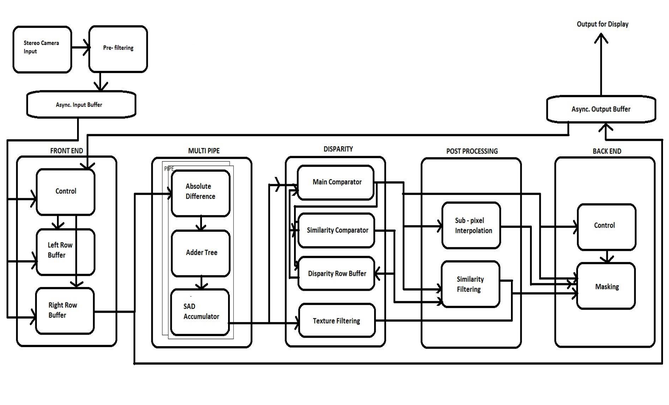
Right Stereo Image



Disparity output image

MATLAB simulations were used to validate the model and to investigate the effect of the iteration steps.

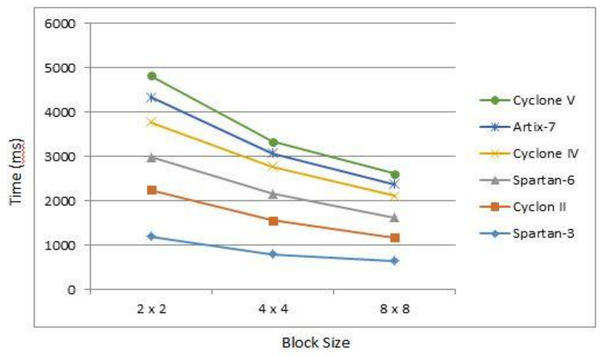
After Algorithmic verification Architecture was implemented on Altera-DE1 board.

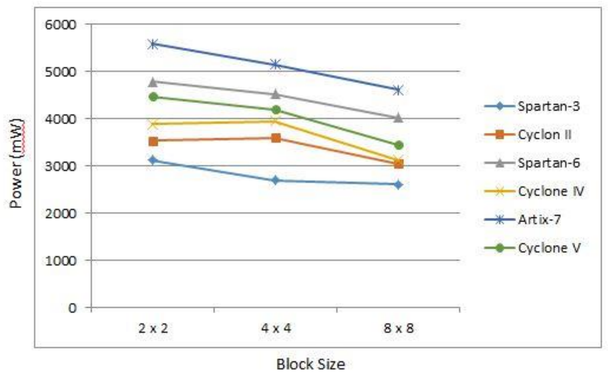


Results

Processing time comparison

Above graph shows the comparison of processing time for Altera and Xilinx FPGA platforms for different image size.





For equivalent FPGA configuration, Altera FPGA development board performs faster than Xilinx FPGA board (except Spartan 6) and also consumes less power.

Conclusions

A relatively time efficient and effective stereo matching algorithm has been implemented that analyses gray scale images to estimate the disparity map. This has been achieved by detecting the correspondence in the stereo images and calculating the disparity values. A large amount of stereo vision applications require quicker computation of dense stereo disparity. To address the issue, the technique implemented enables to achieve the results in desired time frame.

Key References

[1]. FPGA Design and Implementation of a Real-Time Stereo Vision System by: S. Jin, J. Cho, X. D. Pham, K. M. Lee, S.-K. Park, M. Kim, and J. W. Jeon, Member, IEEE.

[2]. Stereo Vision Algorithms for FPGAs By: Stefano Mattoccia, Department of Computer Science and Engineering, University of Bologna.

[3]. A taxonomy and Evaluation of Dense Two-Frame Stereo Correspondence Algorithms By: Matthew Wilhelm, CS5331 Mobile Robotics.

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For further information

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MATLAB code, simulation files, system files are available upon request.