Spring 2012 MSEE Project Presentations

Track	Section	NAME	TITLE	ADVISOR	TIME
		Track 1- Section 1	Network I	Chair: Mir	
T 1	S 1	Deepak Pandey, Nitesh Nayak	Long Term Evolution (LTE) Handover Using NS3 Tool	Nader Mir	9:00 to 9:25
T 1	S 1	Priyal Palkar	Performance Evaluation of Virtual Local Area Networks	Nader Mir	9:25 to 9:50
T 1	S 1	Deep Sutaria, Vishad Sanghvi	Quality of Service Assessment for Multiple VLANs	Nader Mir	9:50 to 10:15
T 1	S 1	Kushal Shah, Rohan Desai	Analysis of Traffic and Node Mobility over Wi-Fi Networks Using Network Simulator	Nader Mir	10:15 to 10:40
		Track1-Section 2	Network II	Chair: Mir	
T 1	S 2	Siddhant Rai	Performance Evaluation of Transmission Control Protocol (TCP) over WiFi Networks	Nader Mir	10:50 to 11:15
T 1	S 2	Jagadish Reddy Goli, Aditi Chandwaskar	Simulation of Label Switching Networks with Multicast PIM-SM Feature	Nader Mir	11:15 to 11:40
T 1	S 2	M. Thiagarajan	Evaluation of Label-Switching Networks with QoS Provision	Nader Mir	11:40 to 12:05
T 1	S 2	Nachiket Rane, Chia-Wei Yuan	Simulation of Hybrid Networks	Nader Mir	12:05 to 12:30
		Track 1- Section 3	Wireless Network	Chair: Zaragoza	
T 1	S3	Roopesh Pavithran, Ashay S Mohile	Wireless MAC Spoofing	Morris Jones	12:40 to 13:05
T 1	S 3	Shreyas Trivedi, Ankur Paul	Reliability and Flow control of Wireless Sensor Network	Morris Jones	13:05 to 13:30
T1	S3	Vinay Kumar, Jaiveer S. Jhala	Secure Communication in Wireless Sensor Network	Moris Jones	13:30 to 13:55

T 1	S 3	Abhijit S Kulkarni, Nitin Huralikuppi	Cooperative Wireless Networking at the Physical Layer	Robert Zaragoza	13:55 to 14:20
		Track 1 - Section4	Miscellanneous	Chair:Jones	
T1	S4	Keyur Gajjar	Low power, Low noise Delta Sigma Fractional N Frequency Synthesizer	Morris Jones	14:30 to 14:55
T 1	S 4	Nirav A. Chudasama	Hardware Peripheral Virtualization Of Embedded Microcontroller	Morris Johnes	14:55 to 15:20
T 1	S 4	Aditya Joshi	Implementation of an Autofocus Algorithm	Avtar Singh	15:20 to 15:45
T 1	S 4	Kaveri Purandare, Shardul Velapure	Low Cost Frequency Synthesizer	Sotoudeh Hamedi-Hagh	15:45 to 16:10
		Track 1 - Section5			
T1	S5	Harmanpreet Singh Nanda	Design of a Sigma Delta A/D Converter	Sotoudeh Hamedi-Hagh	16:20 to 16:45
T1	S5	Sanjeev Murthy	BCM9POWERAD: Variable Voltage, Power Supply PCB Design - (Thesis)	Sotoudeh Hamedi-Hagh	16:45 to 17:30
T1	S5		Reserved by Prof. Avtar		17:30 to 17:55
		Track 2 - Section1	FPGA Systems I	Chair: Choo	
T 2	S 1	Jain Prateek	FPGA Design of a Background Subtraction Module for Recognizing Moving Objects from Video Sequence	Chang Choo	9:00 to 9:25
T 2	S 1	Vishwala Patil	FPGA Implementation of an Efficient Motion Estimation Algorithm for VP8 Encoder	Chang Choo	9:25 to 9:50
T 2	S 1	Vaibhav Purani	Design of a VP8 Model for Video Streaming and Comparative Performance Evaluation of VP8 and H.264	Chang Choo	9:50 to 10:15
T 2	S 1	Karan Methe	FPGA Implementation of Entropy encoding block for VP8 video codec	Chang Choo	10:15 to 10:40

		Track 2 - Section2	FPGA Systems II	Chair: Choo	
T 2	S 2	Katneni M. Vamsi, Shravan K. Soppi	Efficient hardware implementation of 2D DWT/IDWT for MJPEG 2000	Chang Choo	10:50 to 11:15
T 2	S 2	Maruthi Bathina	FPGA-Based Design of Bump Detection Algorithm for Machine Vision	Chang Choo	11:15 to 11:40
T 2	S 2	Deepthi Sridhara	FPGA Design of Hybrid Transformation and Linear Quantization Algorithm for VP8 Encoding	Chang Choo	11:40 to 12:05
T2	S2	Neelesh Mandhare	Spatial Image Filtering	Morris Jones	12:05 to 12:30
		Track 2 - Section3	FPGA Systems III	Chair: Signh	
T 2	S 3	Shalini Asopa	H.264 Decoder Implementation in FPGA	Avtar Singh	12:40 to 13:05
T 2	S 3	Piyush Sagedo	FPGA Design of a Motion Estimation Block for VP8 Encoder	Chang Choo	13:05 to 13:30
T 2	S 3	Nathaniel Mopas	FPGA-Based Embedded Acoustic Echo Canceller System Design Using Pipelined NLMS Adaptive Filter	Chang Choo	13:30 to 13:55
T 2	S 3	Shw. Thimmegowda	FPGA Implementation of Mersenne Twister Pseudorandom Number Generation	Thuy Le	13:55 to 14:20
		Track 2 - Section4	Power Electronics & Miscellanenous	Chair: Reischl	
T 2	S 4	Heena Thakkar	Binary Control Switching and Power Flow Analysis to Provide Closed LoopControl for the Boost Converter	Peter Reischl	14:30 to 14:55
T 2	S4	Charlton Lau, Serhan Pekel	Low-Voltage Ride-Through Stability Improvement Studies for Grid Connected Wind Turbine Systems	Ping Hsu	14:55 to 15:20
T 2	S 4	Susmit A. Mogarkar, Sagar Chandawale	Improving LTE Performance for Heterogeneous Traffic	Melody Moh	15:20 to 15:45
T 2	S 4	Ravi Jadhav, Rohit Bora	Study of Scalable Network Automation Tool	Robert Zaragoza	15:45 to 16:10

Track 2- Section 5 Circuits and Networks

Chair: Shahab

T2	S5	Muthu Kumar Thangavel	Injection Lock Oscillator for Clock Data Recovery Circuits	Ardalan Shahab	16:20 to 16:45
T2	S5	Sulakshan Taank	PLL ILO modeling in SIMULINK using LC oscillator	Ardalan Shahab	16:45 to 17:10
T2	S5	Shweta Panwalkar	Low noise-Injection locking ring oscillator for high speed Clock and Data recovery circuit	Ardalan Shahab	17:10 to 17:35
T2	S5	Shivam Shelat, Jesal Tarkar	Wireless Sensor Networks to Control Lighting	Morris Jones	17:35 to 18:00