Verification of DDR4 SDRAM Memory Controller

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Introduction

In recent times, in this period of innovation, the requirement for memories has been popular on account of its faster processing, ease, and low power utilization. Alongside various advancements in the market, DDR4 additionally called Double Data Rate fourth-generation has added great features; DDR4 Synchronous Dynamic Random-Access Memory at present is important has some innovative working features. This memory gives us higher unwavering quality, accessibility, and usefulness than other models. In this project, the conformation of the DDR4 memory controller is proposed wherein the memory controller is checked using System Verilog and Universal Verification Methodology. We used all our knowledge and used the concepts learned from various research papers to structure a UVM testbench that would follow all the Reset and Power-up initialization processes to reach the idle stage that makes the DDR4 memory controller communicate. This established communication further helps us to verify the read and write data from the DDR4 model.

Methodology

State Diagram

We followed the state diagram to understand the proper functioning of the DUT. It starts with a power on sequence followed by a reset sequence and then the initialization procedure. DUT works on the setting of various mode registers and then followed by the operation you wish to perform.

Various states can be traversed using the read or write sequences. Also, the pre-charging state is reached after every read or write operation and then which is automatically takes the state to IDLE state.

TEST BENCH

- After understanding of the working of various registers and the initialization process, we used UVM methodology to develop a test bench.
- This test bench had various uvm components in it like environment, agent, top and other needed to verify the DUT.
- Various sequences we generated in the sequence class and sent through the driver to the DUT to initialize the DUT.
- Along with this various timing tasks were defined to properly set the sequences in according with timing specification specified by the specification sheet.

Analysis and Results

Initializing values

A default address is loaded into the Mode register so that we can start the MRS address loading sequence.

The waveforms below show that for what period the Cs_n, CAS_n, A15, WE_n, A14, and RAS_n_A16 should go low to load the address in the Mode registers.

Summary/Conclusions

In this project, we were effectively ready to build up a configurable testbench that is able enough to check the power-up and reset initializing of Micron’s DDR4-1600 SDRAM. We structured a total UVM model comprising of sequence, sequence-item, sequencer, driver, monitor, scoreboard, environment, and test class wrapped under a top module.

Key References


Acknowledgements

We would like to show our sincerest gratitude to Dr. Lili Hi and Prof. Morris Jones from Electrical Dept. who guided us throughout the process and motivating us to complete the project.