**RTL Design & UVM based verification of Palm Associative Memory**

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**Introduction**

Hardware acceleration is the process to increase the efficiency of a computational task using specialized hardware rather than using a general-purpose CPU. The project attempted to create a RTL design of the Palm Associative Memory (Hardware acceleration algorithm). The project involves the development of algorithm specific computational architecture, and algorithm-specific communication scheme (coded in SystemVerilog/Verilog-HDL). Improvements in performance due to the possible distribution of the sub-operations of the algorithm and parallelization will be explored. Moreover, UVM based functional verification platform will be designed for the communication scheme and algorithm to ensure correct functional operation.

**Methodology**

PAM consists of 1 master device, 4 slave devices for computations, and 4 network on chip's (NOC) for data transfer as shown in Fig. 2. Each slave device has its NOC to communicate with the master device. The design is not a high-performance design. The RTL design is modularized and parametrized for easy debugging and expansion. Each block present in Fig. 2, is designed using state machine. Computation shown in Fig. 3 sums up PAM retrieval.

**Testbench Architecture**

After understanding specification and pin level details of PAM, we started developing 4 different CRV UVM based architectures to verify PAM subchip IP. These UVM architectures consists of different uvm components, uvm object and uvm packages. In each testbench the sequence-item consists of required variables to generate random stimulus to verify the design. The generated transactions are converted to pin level and drive to DUT with the help of interface from driver. The pin level activity is converted to signal level in monitor and send it to scoreboard for comparison.

**Analysis and Results**

This VE consists of single agent. This VE to check data integrity after integrating all IPs together.

**Table 1.** shows the required number of clock cycles to complete an operation.

**Table 1.** PAM operation analysis

The master device is connected to 4 slave devices as shown in Fig. 2. After reset master accepts 32 bytes of data in input memory as shown in Fig. 8. After taking the input master sends 32 bytes of data to each slave device as shown in Fig. 9. After receiving a write response from slave-1 it will send data to slave-2 and so on. After the master successfully sends data to all the devices it will send a read request to the slave device after receiving a message response from NOC. It sends a read request to each device one by one as shown in Fig. 10. While receiving data from each slave device it simultaneously sorts the incoming data to store time.

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**Key References**


**Acknowledgements**

We would like to express our deep and sincere gratitude to our project advisor Prof. Binh G. Le for his constant support, constructive criticism, and valuable feedback towards the successful completion of this project. We would like to extend our greetings to Dr. Mazad Zaveri and Dev Metia (Student Alumni) from the School of Engineering and Applied Science-Ahmedabad University, for providing helpful insights during the RTL design of this project. Also, the facilities provided by the Electrical Engineering department of San Jose State University to access the lab remotely via Virtual Private Network amidst the global pandemic are invaluable. Our sincere thanks to Dr. Binso Sirkaci, Prof. Morris Jones, and Dr. Thuy Le (Head of the Electrical Engineering Department) for providing us with the golden opportunity to study, learn and execute our knowledge using the skill nurtured and developed during the Master’s Program.