The designers design the SRAMs (Static Random-Access Memory) to meet two needs: providing a direct interface with the CPU at speeds that DRAMs can’t match and integrating DRAMs in systems that need to be highly power efficient. The SRAM serves as cache memory in the first role, bridging the gap between DRAMs and the CPU. Low-power applications are the second driving force for SRAM technology. Since the DRAM refresh current is many orders of magnitude greater than the low-power SRAM standby current, SRAMs are used in most portable equipment in this situation. The project aims to improve the SRAM's overall efficiency by implementing CFET architecture and providing the best PPAC (Power, Performance, Area, Cost) in the memory world. FinFETs are most likely at the verge of their life cycle of scaling. Samsung has moved with Horizontal Nanosheet (HNS) at 3nm. TSMC is going to use FinFET but with a new architecture below 3nm. Intel uses FF for 7nm and will likely move with HFS for 5nm. As Figure 1 shows, the industry’s roadmap is FinFET to HNS using Fork sheets or not, and there is a smooth transition to CFET.

The project had three phases. The first phase of the project was to get familiarized with the complete process flow and device simulation of 25 nm 2D single layer six transistor SRAM cell with the help of a workbench using Sentaurus TCAD. The device’s electrical characteristics were simulated in three dimensions using Sentaurus Device and plotted using visual, as shown in Figures 4 and 5.

The second phase of the project involved mask modification of fin layers, 6T, 8T and an 3D stack SRAM cell using IC validator and ICWBEV Plus. I modified the process flow to support two layers (Player on top of the N layer) structure generation in the S PROCESS.

The final phase of the project covers designing a CFET 6T SRAM cells including complete process flow and layout creation.

Major Steps During Process Flow & Layout Creation:
1. Layout creation and Mask Separation; Separated N and P layer (Poly, Fin, Line) and integrated them together in the flow.
2. Source Drain Implantation; Modified the code accordingly to do P type implantation separately as N type implantation. Tweaked the masking of PWELL and NWELL while diffusing material such as Boron for P type and Arsenic for N type.
3. Buffer creation: I have separated top layer with bottom layer using oxide layer thickness of 10a.
4. Fin Creation: fins were created on top of oxide buffer alone without substrate layer attached.
5. Pocket Formation: Diamond shaped pockets were formed on top layer by modifying proc to changing the measurements with reference coordinates in X directions.
6. Other process flow such as deposition, etching, mask formation with referenced position were also changed accordingly to meet desired structure as shown in the Fig 12.
7. Last but most important action that I did was routing of the entire design using 7 layers M1 M2 and Contact and integrated N layer to P layer using Copper.

In general, the project entails the generation, design and construction of various 3D layout blueprints of separate SRAM cells, such as 6T, 8T on the basis of laying the gro undwork for future memory devices to solve one of the most difficult problems of the 2030 era. The project targets to meet upcoming device technology. The flow can be modified to achieve desired device for other CFET memory applications.

Key References

Acknowledgements
I would like to especial thank my supervisor, Dr. Hiu Yung Wong, for his guidance and support throughout my master’s degree. And I'm so grateful he was my teacher. His insights and discussions about the problems were of immense help. I don’t have enough words to say how thankful I am that he was my mentor. I like his teaching “The teachers open the door, but you must enter by yourself”.

In all my endeavors and accomplishments, the love and support I have received from my parents and brother can never be thanked enough.