System Verilog Verification of OFDM Communication System with UVM
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Introduction
OFDM, Orthogonal Frequency Division Multiplexing is a form of multicarrier modulation. OFDM generates a group of closely spaced modulated carriers called OFDM signal. OFDM modulation techniques place the stream of high data rate onto many slowly modulated narrowband closely spaced subcarriers. OFDM signal contains all the data signals that need to be separated by some amount of carrier space so that the receiver can effectively demodulate the OFDM signal. This carrier spacing is set to reciprocal of symbol period (total period of OFDM signal).

In this project, verification is performed on Inverse Fast Fourier Transforms (IFFT), Pilot-based algorithm, and Quadrature Phase Shift Keying (QPSK) algorithms of the OFDM scheme. The verification environment leverages the Universal Verification Method. Verification includes generation of sequences to stimulate the Design Under Test (DUT), input and output monitor to observe the pin level activities on the DUT, driver to send the generated sequences on the DUT, scoreboards to capture and process the pin level information from input and output monitors, active agent to encapsulate driver, monitor, and sequence for OFDM transmitter interface, environment to create the agent class and make analysis port connections, test to start and stop the simulation, and top-level module to instantiate the test. In this project, the black-box approach for verification is used for verifying the OFDM transmitter design. We also have used GTWave analysis and UVM standardize messaging to determine the functional correctness of the DUT.

OFDM UVM Verification Environment
Top Level Module
The top level module is where we define our uvm_pkg.*. The UVM package contains all the information about the derived classes, base classes, UVM factory, utility macros. Hence it is a type of a super-parent class which contains all the information. After defining the UVM package, we include all the components of our UVM verification environment. Module top is defined in the top-level module, and instances and directions of the interface are provided. The configuration database gets set up in the top-level module.

Test Stimulus
Sequence is where the actual stimulus is, hence all the user defined or engineer created stimulus which goes on to the DUT is created. The engineer has to generate the stimulus with random constraints, as it is not possible to generate the whole stimuli. The sequence is extended by uvm_sequence. The value of data_in is given in the code, and the last two bits are manipulated using inline constraints. Hence various values if data_in are given to the stimulus, which then goes to the DUT via the driver, and thereafter the outputs are compared with the actual values of the DUT in the predictor model of a scoreboard.

The stimulus that is generated in the UVM sequence is driven to the DUT via the UVM Sequence Item. The specified data objects that are to be driven to the DUT are called sequence items. The Sequence item is extended by uvm_sequence_item. Sequence items are generated using System Verilog constraints for randomization.

Simulation Result and Waveforms
The attached screenshots are the results after simulating the UVM verification environment on the DUT. This simulation is running on the platforms Synopsys VCS and EDA Playground as well. The waveforms are also generated using EPIWave and are attached below.

The Simulation result attached below shows the comparison between the actual value and predicted values made in the scoreboard. If the DUT passes the test case, the scoreboard will print the message that the DUT has passed the test otherwise the scoreboard will print the message that this particular test on the DUT is failed.

References

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