Ansys PCB simulations for EV WPT Charging

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**Introduction**

With the global push to accelerate the mass adoption of electric vehicles (EV), there has been a renewed focus on addressing some of the drawbacks of EV, such as reducing the time required to charge an EV battery. The most common charging method for the majority of EV involves connecting a plug-in cable that is tethered to a charging station. These charging stations require the EV to be immobile while the battery is charging. These down time can be avoided with the implementation of wireless power transfer (WPT) charging.

![Figure 1. Basic Configuration of an EV WPT Charging System.](image1)

A simplified static WPT charging system diagram is shown in Figure 1. Starting from the ground side, the WPT system would be sourcing power from the grid. In which the AC voltage from the grid would go through an AC/DC converter. The output DC voltage would then get converted from DC voltage to a high frequency AC voltage. This high frequency AC voltage would go through a compensation network that enable maximum WPT at the desired resonant frequency through a transmitter coil. On the vehicle side, a receiver coil would receive the wireless power and that will go through another compensation network to provide a constant oscillating AC voltage. This voltage would then go through an AC/DC converter to provide a constant voltage to charge an EV battery pack.

![Figure 2. PCB Block Diagram.](image2)

The basic WPT configuration will be reconstructed by manufacturing six PCBs and assembly all of them together as shown in Figure 2. The system consists of one Transmitter (Tx) board, one Receiver (Rx) board, and four isolated gate driver boards.

**Methodology**

**Isolated Gate Driver Board**

The purpose of the isolated gate driver board is to power the H-Bridge inverter and H-Bridge rectifiers that are present in the Tx and Rx PCBs. The gate driver board utilizes a TI UCC21520 isolated dual-channel gate driver IC, which provides 5.7 kV voltage isolation between the input and to the output channels. The isolated gate driver board was also designed to be on an interchangeable circuit card for the flexibility of testing different gate driver ICs.

![Figure 3. Top and Bottom View of Isolated Gate Driver Board](image3)

**Transmitter (Tx) / Receiver (Rx) Boards**

Both the Tx and the Rx PCBs will each house half of the basic configuration of a dual sided LCC resonant converter as shown in Figure 4.

![Figure 4. A dual sided LCC resonant converter.](image4)

The Tx board will consist of an Inverting H-Bridge switching network that will be controlled by two isolated gate driver boards. The high frequency AC voltage output will then go through the LCC resonant tank and transmit through the Tx coil. For the Rx board, the Rx coil will receive the wireless power and compensate the power through a LCC resonant tank that feed that power to a Rectifying H-Bridge switching network that will be controlled by another two isolated gate drivers.

![Figure 5. Top view of the Tx Board with two isolated gate driver boards connected.](image5)

**Analysis and Results**

For any PCB, its power distribution network consist of multiple elements such as copper traces, copper planes and vias. Each one of these required elements for a multi-layered board have a some minimal resistance tied to them, which equates to some power loss. Using Ohm’s law:

\[ P_{loss} = I^2 	imes R \]

where \( I \) represents current and \( R \) is the sheet resistance of the pcb element in question, the power loss per pcb element can be calculated. However, to calculate and add up all the power losses present on the gate driver board with heatsinks will react long. That is where we will be utilizing the calculating power of Ansys software to provide the current and density plots to show us what parts of the layout of the gate driver and the Tx board will have to be redesigned to avoid excessive voltage drops or current choking points. With the generated power density plots, data will be utilized in Ansys Icepak to identify potential hot spots on the board.

![Figure 6. Power density and temperature rise plots of the initial PCB design.](image6)

**Isolated Gate Driver Board Anslysis Results**

The initial PCB design for the gate driver board that was submitted to Ansys, was a 4-layer board with only 0.88 oz. of copper per layer.

![Figure 7. Power density and temperature rise plots of the redesigned PCB design with 4-oz. of copper per layer.](image7)

To address the issues found in Figure 6, the copper shapes and traces for the areas that were identified to have high current and power density were increased in size. Also increasing the copper stack up thickness from 0.88 oz. to 4 oz. for each conductor layer assisted in alleviating the heat dissipation within the board as seen in Figure 7.

**Conclusion**

By leveraging Ansys simulation software, I have a better understanding of how a PCB layout design can impact the performance of a circuit and improve upon the three WPT PCB designs before even having to assemble a physical prototype.

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**References**
