The data center industry is headed towards lower point of load voltages with increased load demands contributing to higher IR losses in power busses. Raising the bus voltage from 12V to 48V is a popular area investigated today for reducing power delivery Losses. Switched Capacitive Converters (SCCs) are a popular topology used for this purpose. However, SCCs suffer from low tolerance for operating conditions and are unregulated. The proposed Multi Resonant Switched Capacitor Buck Converter (MRSCBC) can resolve these challenges while also providing output regulation. Switch Mode Power Supplies exhibit high EMI noise and with an increased number of switches in an MRSCBC, controlling EMI noise and compatibility is essential. This proposal will focus on the use of PCB design and software simulations to optimize EMI losses and parasitic elements in the resonant circuit to improve the robustness of an MRSCBC.

Texas Instruments’ LM5141 synchronous buck controller featuring peak current mode control provides feedback closed-loop control signals to two UCC21520 isolated Gate Drivers per phase. Featuring a buck converter on the output of the multi-resonant switched capacitive converters allows the use of traditional synchronous buck controllers. Traditional control ICs simplify the design of the feedback control and allows for flexibility in choosing controllers as the synchronous buck controller with peak current mode control is common. The Isolated Gate Drivers help reduce switching losses while each driver gates. The image below shows the output voltage of the spice design.

For the PCB design, the component layout chosen focuses on controlling EMI by featuring two ground planes and a focus on linear layout and power flow. A 6-layer, design is needed to route the signals. An Image of the initial design is shown above.

For the design and analysis, suitable components for the design using SPICE simulations are needed. As shown in Table 1, parasitic components are modeled. The self and mutual parasitic capacitance, inductance, and resistance are exported as Cadence Capture PSpice files. The PCB model is imported into Ansys Q3D that extracts a model for the self and mutual parasitic capacitance, inductance, and resistance and exports it as a PSpice file. The PSpice model is imported into Spice. Q3D extracts a model for the self and mutual parasitic capacitance, inductance, and resistance and exports it as a PSpice file. The PSpice model is imported into Spice. This Power Conversion: A Review," in 2020 IEEE Texas Power Engineering Conference and Exposition (TPEC), College Station, TX, USA, 2020.

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Analysis through ANSYS Electronic Desktop allows for the simulation of the operation of the design close to experimental data and provides feedback on improvements before the design is completed. An acceptable inductance range value in the gate drive and switching traces is presented for the operation of the MRSCBC. Future work constitutes an experimental prototype of the proposed converter to validate the system’s effectiveness and highly efficient characteristics.

### Methodology

**Components**

- **Input DC Voltage**: $V_i = 48V$
- **Output DC Voltage**: $V_o = 12V$
- **Switching Frequency**: $f_s = 500 kHz$
- **Output Current**: $I_o = 125 A$
- **Output Power**: $P_o = 1.5 kW$
- **Flying Capacitor**: $C_{fly} = 12 nF$
- **Middle Capacitor**: $C_{mid} = 100 nF$
- **Output Capacitor**: $C_{out} = 100 nF$
- **Resonant Capacitor**: $C_r = 1 nF$
- **Resonant Inductor**: $L_r = 10 nH$
- **Output Inductor**: $L = 22 nH$
- **Resistor Load**: $R_o = 96 mΩ$
- **Deadtime**: $t_d = 10 ns$

**Analysis and Results**

Q3D extracts a model for the self and mutual parasitic capacitance, inductance, and resistance and exports it as a PSpice file. The PSpice model is imported into Ansys Q3D which provides the values of the parasitic components at the switching frequency, 300 kHz in this case. The self and mutual inductance and capacitance matrix is then imported into Cadence Capture as a square model. Analysis of the performance of the converter with a parasitic model finds that the inductance is the most sensitive variable in design. Acceptable maximum inductance values range from $L \times 10^{-11}$ to $L \times 10^{-12}$. Higher inductance values in the inductor range in the control and gate drive traces produce voltage spikes during rising and falling edges high enough to block the MRSCBC from starting or reaching 12V output.

The bottom figure below shows the startup response with original and reduced inductance values. From left to right, the figure shows first failure to startup due to high inductances. The second portion shows startup once inductances are reduced in the gate drive circuits but large voltage spikes. Third portion shows startup with controlled voltage spikes due to lower inductances in control and gate drive circuits. The parasitic model highlights the importance of reducing the inductance in the control and gate drive traces in the PCB design. The MRSCBC redesign to lower inductances is shown in the last image.

The multi-resonant power converter circuit however is tolerant to the aforementioned inductance values.

### Key References

