Verification of DDR4 Memory

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Introduction

Memory is an integral part of a computer system. The next-generation memory market aims to adopt new technologies, capable of achieving higher performance at low power consumption. Thus, verifying a DDR4 memory seemed to be an exciting challenge and a great learning opportunity to us. We aimed to use our understanding of Design Verification concepts, UVM and System/Verilog in this project to develop a reusable base environment using which various configurable memory’s can be verified. The DDR4 memory device requires a set of RESET, Power-Up and Initialization procedure to get itself into a state from wherein different READ/WRITE operations can be performed and then verified. We developed a testbench architecture using Universal Verification Methodology (UVM) which can provide those RESET and Power-Up procedures to set up the memory device.

Methodology

The device has seven Mode Registers to program application flexibility, various functions, features and modes. The user-defined variables can be programmed into these registers using MODE REGISTER SET (MRD) Commands.

The above state diagram helps to understand the working of DDR4 memory device. There are different commands used to move from one state to another. We have developed the environment which brings the memory device into the Idle State as shown in the diagram. Using the ACTIVATE Command various READ/WRITE operations can be performed.

TESTBENCH ARCHITECTURE

After acquiring the understanding of the working of memory device from the specification sheet, we developed an architecture comprising of various UVM components and objects each serving a specific purpose. We developed packages for defining various enumerations and structures. The sequence and sequence-item class contain the required variables which were used to create various scenarios.

Analysis and Results

To ensure the set up of the memory device we made sure that the RESET and Power-up sequence required was implemented correctly as per the specification sheet.

The above waveform ensures proper handling of the RESET_N, CK CKE signal along with the required timing constraints.

Next, we made sure that Mode Registers were programmed in a correct format for the device to reset and power up properly. The above diagram shows the sequence in which the mode registers were programmed.

Each mode register allowed us to program the memory device’s different functionality, features and modes of the x4 device. So we even analyzed the bit fields of each register and verified correct value was programmed into a particular register in order for the device to work.

Taking an example of the Mode Register 0. This would help determine the Burst Length, Burst type, CAS latency, WRITE recovery time and MR select. The above diagram depicts the settings that are required for Mode Register 0 for setting up the device.

Summary/Conclusions

In this project we were successfully able to develop a configurable testbench capable enough to verify the power-up and reset procedure of Micron’s DDR4-1600 SDRAM. To verify the memory’s initial reset and power up procedure we developed a Physical Configuration Component for handling the timing requirements of the design.

The environment we developed in this project can be used as a base to test various flavors of the DDR4 memory by changing the configuration in DUT config class.

Key References


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