Design of Low Power Sigma Delta ADC
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Abstract
Analog to digital converters (ADC) play an important role to interact with the signals around us. The design of reliable ADCs in terms of low power, high resolution, and low cost are in demand. With the advancement in the technology and methods of converting signals, several architectural techniques have been proposed. A Sigma-Delta ADC is one such method used for signal conversion. This project concentrated on the design of converter for audio-applications where the design exploits the concept of oversampling and noise-shaping. The Sigma-Delta ADC consists of two major blocks: modulator and a filter. The project is focused on designing a modulator in 45nm technology with 1.8V supply voltage. The designed modulator consists of a voltage reference circuit, an integrator which is based on the switched capacitor concept, voltage comparator, and 1-bit DAC. The designed modulator achieved the resolution of 11 bits and the overall power consumption is 0.58mW. This low power, high resolution, and less area make Sigma-Delta modulator a good choice.

Keywords: Sigma-Delta ADC, oversampling, noise-shaping, low power.

Introduction
The world is technology driven. With the advancement in technology, digital signal processing of the data has become faster and cheaper. The CMOS technology lead the new dimension in the development of the DSP and with this case, the data storage is mostly digital now. In contrast to this, the signals we interact in nature are analog. One needs a way to interact with the analog signals, understand the way these signals behave and fetch the data. The circuit used to convert signals from analog-to-digital is called as an analog to digital converters (ADC). As the world is digital now, the market expects a design of low power consumption products[1].

Figure 1: Block diagram of Nyquist ADC (left) and Over sampling ADC (right)

In broader sense, ADC techniques can be classified into two types based on sampling frequency. The first type is called Nyquist type ADC where, fs ≥ 2B, and figure 1 shows the block diagram of Nyquist type. On the other hand, the second type of ADC’s are termed as the oversampling ADC (are also termed as sigma-delta ADC) where, fs > 2B[2]. The above figure 1 shows the block diagram of over sampling ADC.

Methodology
The project uses the over sampling concept and focused on designing second order sigma-delta modulator (SDM). Based on the order of the transfer function a modulator can be designed. The first step is to know the overall block diagram and what constitutes a second order SDM.

As can be seen in the figure (figure 2), this architecture consists of 2 integrators connected back to back and first integrator accepts the differential input and output is given to the next. Followed with a comparator, which is acting as 1-bit ADC and provides digital data. Finally, a 1-bit DAC is used in the feedback path.

Figure 2: Block diagram of second order SDM

A transistor level design is carried out for each block mentioned above and are analyzed to obtain desired results. Then a layout design is carried out to determine the total area occupied by the modulator block.

Analysis and Results
Voltage Reference: The concept of current mirror is used in the beta-multiplier design and a constant current, independent of supply voltage is generated. Applying the KVL in the loop where the resistor R is present and solve for the current I, we have

\[ I = \frac{V_{in}}{R} \]

From this equation, we can see that the current I is independent of supply voltage and a beta multiplier thus acts as a self-biasing circuit. A start up circuit, beta multiplier and high swing cascading concept is used to generate constant reference voltages and schematic is shown in the figure 3.

Operational Amplifier Design: An amplifier is a circuit which provides an amplified version of the input signal. A folding of one structure into another along with providing cascode will give high output swing, high output impedance, high gain and high bandwidth[3][4]. The gain of the amplifier is given by,

\[ A_p = \frac{V_{out}}{V_{in}} \]

The following figure shows the schematic view and simulation results of the folded cascode amplifier. The circuit achieved 52.12dB gain, with cut off frequency of 148.55KHz, unity gain frequency of 60MHz, phase margin is about 79° and gain margin is about 45dB. This opamp acts as building block for switched capacitor circuit.

Figure 3: Schematic view of voltage reference

Second order Sigma Delta ADC: All the designed blocks are integrated to get the second order sigma delta ADC. A test bench is created and simulated to get the output waveform and is shown below along with the frequency spectrum plot and image showing ENOB and SNR.

Figure 4: Schematic view of Folded cascode amplifier and simulation results

1-bit DAC: The 1-bit DAC is implemented using a D flip flop (D FF) which uses TSPC (true single-phase clock architecture) [5]. A D FF is a digital circuit, which stores a value until it is triggered by an edge of the clock at the clock input, if D input is changed output changes or else flip flop holds the previous value. The schematic view is shown below.

Figure 5: Schematic view of comparator and simulation results

Figure 6: Schematic view of 1-bit DAC

The consolidated results are shown in the table below.

<table>
<thead>
<tr>
<th>Table 1: Achieved design specifications</th>
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<tbody>
<tr>
<td>Parameter</td>
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<tr>
<td>Clock Frequency</td>
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<td>Signal Bandwidth</td>
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<td>Total power consumption</td>
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<tr>
<td>Total area occupied by the modulator</td>
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Layout Design: Using cadence layout editor, layout design of each block within the modulator are carried out and verified for LVS and DRC. Finally these blocks are integrated to get the second order SDM. The total area occupied is 110um x 85um.

Figure 7: Testbench setup for sigma delta ADC, simulation results, and image showing ENOB and SNR

Conclusions
The project is focused on designing the second order Sigma-Delta ADC. Both circuit and layout were designed based on the targeted constraints. As the project is intended for audio applications, an input signal of 20KHz frequency, and a sampling frequency of 3.2MHz is selected which will give rise to over sampling ratio as 64. The designed circuit was able to achieve 68dB SNR and 11 bits of ENOB. The total power consumption by the circuit is 0.56mW, and the total area occupied by the modulator is 110um x 85um. This low power, high resolution and less area make Sigma-Delta modulator a good choice for audio applications.

Key References
[4] Klaus-Jan de Langen, Member, IEEE, and Johan H. Huisings, Fellow, IEEE. Compact Low-Voltage Power-Efficient Operational Amplifier Cells for VLSI.
[5] Rishi Ratan “Design of A Phase Locked Loop Based Clocking Circuit For High Speed Serial Link Applications” University of Illinois at Urbana-Champaign, 2014

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