Introduction

The objective of this project is to modify the DSP blocks on current FPGA and create an enhanced version with the metrics comparison between FPGA series and families. So in this project, we designed an advanced DSP block that efficiently performs 2 (8-bit) i.e. 18-bit and 4 (4-bit) i.e. 16-bit multiplication and compare the performance.

- The design was implemented using parametrizable pipelined MAC for both baseline DSP and enhanced version.
- Firstly, a pipelined parametrizable MAC was designed and simulated followed by the design and implementation of baseline DSP block.
- After, this design enhanced version of baseline by modifying the 9-bits and 4-bits multiplier. We measured the performance improvement by using this improved DSP block on different versions of FPGA series and families.
- Results show that baseline DSP block took 14 clock cycles of maximum clock frequency to release the first output of MAC, while enhanced version of DSP took only 11 clock cycles quantifying the performance by 21%. The overall power consumption decreased by 8% and memory utilization increased by 0.2%.

Problem Statement: The project overcomes the issue of limited number of multiplier packings on current FPGAs.

Methodology

Multiply and Accumulate (MAC)

The flow of the project starts with the design and implementation of the Multiplier and Accumulator (MAC) that computes the multiplication and addition of the fixed-point numbers with pipelined stages. The MAC design consists of two main blocks which have their own circuitry.

- One block will perform the multiplication.

While other one preforms fixed point addition.

Steps Followed:
- Signed Multiplication of two numbers along with partial product generation.
- Storing the product in accumulator.
- Adding the newly generated product and stored value.

Baseline DSP Block

Within this study, we introduce as a reference an Arria-10-like DSP block, to which we compared our updated DSP block.

For multiplication the input is divided as following:
- Y2 is divided into two halves, i.e. Y2(M5) and Y2(L5).
- Y2(M5) is multiplied with the X2 using M4.
- Y2(L5) is multiplied with the X2 using M3.

Features:
- DSP reference model enables 27-bits multiplication, which can be divided into two 18-bits multiplication.
- The DSP framework is identical to Arria-10 and Stratix-10 processor without floating point calculation functionality.

Enhanced DSP Block

The enhanced version of DSP block is the modifications to the basic reference block using 9’9 and 4’4 multiplier MAC modes.

- M1: 18’18-bits
- M7, M8, M5, M6 for 4’4-bits multiplication
- M3 and M4 for 9’18 bits
- M2: 9’9-bits multiplication
- One more compressor C4 is used and incorporated at the early stage after M7 and M8 multipliers.

Analysis and Results

The waveform shows the starting operation of MAC when load is 1. Each cycle multiplication occurs and stores the value in accumulator followed by addition of new product and acc value at next cycle.

The improved DSP block takes 11 clock cycles to produce the result whereas the baseline DSP block takes 14 clock cycles. Thus the speed of the enhanced DSP block increased by 21%

Power Consumption Analysis

- Baseline DSP Output after 14 clock cycles
- Enhanced DSP Output after 11 clock cycles

After simulating in Quartus II for various versions of FPGA families, we observed that the improved DSP block shows 8% power reduction on average.

Summary/Conclusions

- Relative to the standard DSP block it can handle twice as many 9-bits and four times as many 4-bit multiplications and MACs.
- We measured the performance improvement by using this improved DSP block on different versions of FPGA series and families.
- Baseline DSP block took 14 clock cycles to release the first output of MAC, while enhanced version of DSP took only 11 clock cycles quantifying the performance by 21%.
- The overall power consumption decreased by 8% and memory utilization increased by 0.2%.

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