Verification of SDRAM Controller on Wishbone Bus

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Introduction

The proposed project is mainly focused on Functional verification and Performance evaluation of a SDRAM Memory controller with the Wishbone interface. A memory controller is an essential element in the memory system that is mainly used to read, write and generate refresh cycles on the Memory. It is involved in most data paths of an SoC. The main memory of the computer is made of DRAM cells that must be refreshed periodically otherwise; the data is lost. The memory controller efficiently performs read or write data and fresh DRAM cells. The main objective of this project is to verify the read-write operations and check for the periodic generation of refresh cycles by the memory controller. Also, the performance of the DRAM system is analyzed. Therefore, it is essential to provide an optimized solution by creating an environment to achieve full coverage. The verification method is based on the UVM environment that can be reused later. The statistical data is gathered to analyze the performance of the memory controller.

Today there are more and more functionalities implemented within a memory controller that is integrated either within the motherboard or the Central Processing Unit. It is a cumbersome task to verify such large SoCs. The verification of the memory controller is based on the UVM environment that can be reused late. A UVM framework is based on System Verilog language which is object-oriented programming language. This helps in constraint random verification with implementation of code coverage and asserts. This project proposes a methodology for verifying a Wishbone amenable Memory controller core. It is essential to provide an optimized solution by creating an environment to achieve full coverage.

Methodology

Dynamic Random Access Memory

A DRAM uses a Metal-Oxide semiconductor technology. It is used as the main memory in the computer systems. It consists of a capacitor and an access transistor. The capacitor can store charge or discharge it. It can store a bit 0 or bit 1. The access transistor acts as a switch. If the capacitor is charged, it is implied that the charge stored is Logic 1. Similarly, if the capacitor is discharged the charge stored is Logic 0. A DRAM cell is a simple chip where the silicon chips are densely packed, and this makes the chip not expensive.

Testbench Results

The SDRAM used for our project is of the size 64Mb. It has 67,108,864 bits. It is a high-speed CMOS DRAM. It has an asynchronous interface with 4 banks. Each bank in the SDRAM has 8192 rows and 2048 columns of 4 bits. Read and write access are in the form of bursts. Access begins with ACTIVE command, then the READ or WRITE operation is done. The SDRAM provides burst length of 1, 2, 4, 8 and Full-page.

Performance Calibration

Efficiency comparison for open and closed row

Efficiency comparison between banks

Summary/Conclusions

There are several components in a computer system and memory plays a very important role. It is the heart of the processor. They are of several types like the CPU Registers, SRAM, DRAM Disk etc. [4] The memory controller controls major functionality of handling the transactions between the CPU and the main memory. In this project we have verified two features of the memory controller and measured the performance of the controller. We can conclude that the memory controller is able to send refresh signals within 15,625us but sometimes it takes more time when its busy performing read an write transactions.

Key References


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